# Evaluation Board User Guide <br> UG-205 

## Evaluation Board for the ADP 1850DP Step-Down DC-to-DC Controller

## FEATURES

Input range: 10 V to 15 V
Output voltage: 1.09 V
Output current: 50 A
Switching frequency: 300 kHz
Operates in PWM
Compact, low cost, and efficient design

## EVALUATION BOARD DESCRIPTION

This document describes the design, operation, and test results of the ADP1850DP-EVALZ operating in dual-phase mode. The input range for this evaluation board is 10 V to 15 V , and the regulated output voltage is 1.09 V with a maximum 50 A output current. A switching frequency ( $\mathrm{f}_{\text {sw }}$ ) of 300 kHz is chosen to achieve a good balance between efficiency and the sizes of the power components.

## ADP1850 DEVICE DESCRIPTION

The ADP1850 is a dual-channel, step-down switching controller with integrated drivers for external N -channel synchronous
power MOSFETs. The two PWM outputs are phase shifted $180^{\circ}$, which reduces the input RMS ripple current, thus minimizing required input capacitance. The two outputs can be combined for dual-phase PWM operation that can deliver more than 50 A output current. The internal parameters of the two channels are optimized for current sharing.

In addition, boost diodes are integrated into the ADP1850, thus lowering the overall system cost and component count. The ADP1850 can be set to operate in pulse skip, high efficiency mode under light load or in PWM continuous conduction mode.
The ADP1850 includes externally adjustable soft start, output overvoltage protection, externally adjustable current limit, power good, tracking function, and a programmable oscillator frequency that ranges from 200 kHz to 1.5 MHz . The ADP1850 provides an output voltage accuracy of $\pm 0.85 \%$ from $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and $\pm 1.5 \%$ from $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ junction temperature. This controller may be powered from a 2.75 V to 20 V supply is available in a 32 -lead $5 \mathrm{~mm} \times 5 \mathrm{~mm}$ LFCSP package.


Figure 1.

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## COMPONENT DESIGN

For information about selecting power components and calculating component values, see the ADP1850 data sheet.

## INDUCTOR SELECTION

A $0.47 \mu \mathrm{H}$ inductor with a 50 A saturation current rating and a 30 A average current rating ( 744355147 from Würth Elektronik) is selected. This is a compact inductor with an iron alloy core, which offers high performance in terms of low $\mathrm{R}_{\mathrm{DC}}$ and low core loss. An alternative to the 744355147 is the SER1408-301M ( 300 nH with about 40 A in saturation current and average current rating) from Coilcraft. If higher efficiency or lower DCR is desired, choose a physically larger inductor with approximately the same inductance value.

## INPUT CAPACITORS

Because of the large input current ripple requirement, four $180 \mu \mathrm{~F} / 16 \mathrm{~V}$ OS-CON ${ }^{\mathrm{wt}}$ capacitors have been selected for the input bulk capacitance. In addition, one MLCC decoupling capacitor $(10 \mu \mathrm{~F} / 25 \mathrm{~V})$ is used at each of the high-side MOSFET.

## OUTPUT CAPACITORS

A total of six $560 \mu \mathrm{~F} / 2.5 \mathrm{~V}$ OS-CON" capacitors is used at the output. These aluminum solid capacitors with conductive polymer have low ESR and high current ripple rating. In addition, four $47 \mu \mathrm{~F}$ MLCCs are added for filtering out the high frequency voltage ripples.

## MOSFET SELECTION

For low output or low duty cycle, select a high-side MOSFET with fast rise and fall times and with low input capacitance to minimize charging and switching power loss. As for the synchronous rectifier (low-side MOSFET), select a MOSFET with low $R_{D s o n}$ because the switching speed is not critical and there is no switching power loss in the low-side MOSFET.
For the high-side MOSFETs of each channel, two BSC080N03LS connected in parallel from Infineon Technologies in the PG-TDSON-8 or Super-SO8 package are selected. This part has low input capacitance ( 1.2 nF ) and fast transition time ( 3 ns ). For the low-side MOSFET, two BSC030N03LS connected in parallel, with $R_{\text {dson }}$ of $4.7 \mathrm{~m} \Omega$ at a $\mathrm{V}_{\mathrm{GS}}$ of 4.5 V , are selected.

## TEST RESULTS



Figure 2. Efficiency


Figure 3. Line Regulation


Figure 4. Load Regulation


Figure 5. Output Ripple, 50 A Load


Figure 6. Step Load Transient, Vout

## EVALUATION BOARD OPERATING INSTRUCTION

1. Connect Jumper J3 (EN) to the high position to enable Channel 1 and Channel 2 of the ADP1850. Jumper J3 is connected to both EN1 and EN2.
2. Connect Jumper J4 (FREQ) to the low position for 300 kHz operation.
3. Connect Jumper J1 (SYNC) to the high position for PWM operation.
4. Connect the positive terminal of the input power supply to the input terminal, T 1 . The input range is 10 V to 15 V .

Table 1. Jumper Description

| Jumper | Description | Default Factory <br> Setting | Function |
| :--- | :--- | :--- | :--- | | J1 | SYNC | High | Connect high for PWM. For synchronization to an external clock, run the external clock <br> source to this pin. <br> Connect high to enable Channel 1 and Channel 2 of the ADP1850 or low to disable both <br> channels. <br> Connect low for 300 kHz or high for 600 kHz operation. This 50 A evaluation board is configured <br> for operation at 300 kHz Connect J4 low. |
| :--- | :--- | :--- | :--- |

Table 2. Performance Summary ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| Parameter | Condition |
| :--- | :--- |
| $\mathrm{V}_{\text {IN }}$ | 10 V to 15 V |
| $\mathrm{f}_{\text {Sw }}$ | Switching frequency, 300 kHz |
| Vout $^{\text {lout }}$ | 1.09 V |
| Vout Ripple, DC Load | 0 A to 50 A |
| Vout Deviation upon Step Load Release | 16 mV at 50 A load |

## OTHER INFORMATION ABOUT THE EVALUATION BOARD PCB LAYOUT

As seen in Figure 1, the layout of this evaluation board is not optimized for the smallest PCB area. It is laid out in such a way that any of the components can be desoldered and replaced easily with different components with a hand soldering iron so that the user can modify the existing design without acquiring a new PCB layout. The physical size of the compensation components is 0603, which is selected for its ease of hand soldering when reworking the board is needed. The size of these components can be 0402 or even smaller in the final design. Note that there are extra place holders for input bulk capacitors, output filter capacitors, and MOSFETs. The user
can remove, add, or change any of these power components to achieve a particular design objective. The track functions, where TRK1 and TRK2 are pulled up to VCCO through $0 \Omega$ dummy resistors, are not used on this evaluation board. Also dummy $0 \Omega$ resistors are placed at the driver gates, DHx and DLx, for evaluation purpose only and can be removed in the final design. Furthermore, many test points are placed on the evaluation board so that the user can easily evaluate the performances of the ADP1850 with an oscilloscope. See Figure 7, the evaluation board schematic, for more information.

## EVALUATION BOARD SCHEMATICS AND ARTWORK




Figure 8. Top Silkscreen



Figure 10. Second Layer (AGND Plane)


Figure 11. Third Layer (PGND Layer)


Figure 12. Bottom Layer (PGND Layer)


Figure 13. Bottom Silk Screen

## Evaluation Board User Guide

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 3.

| Quantity | Reference Designator | Description | Manufacturer | Part No. |
| :---: | :---: | :---: | :---: | :---: |
| 1 | U1 | DUT | Analog Devices, Inc. | ADP1850 |
| 4 | CIN10, CIN13, CIN20, CIN23 | OSCON, $180 \mu \mathrm{~F}, 16 \mathrm{~V}$ | Sanyo | 16SEP180M |
| 4 | CIN11, CIN12, CIN21, CIN22 | MLCC, $10 \mu \mathrm{~F}, \mathrm{X} 7 \mathrm{R}, 25 \mathrm{~V}$ | Murata | GRM32DR71E106KA12 |
| 4 | CSS1, CBST1, CBST2, CVIN | MLCC, $100 \mathrm{nF}, \mathrm{X} 7 \mathrm{R}, 25 \mathrm{~V}$ | Murata | GRM188R71E104KA01 |
| 2 | CV5, CDR | MLCC, $1.0 \mu \mathrm{~F}, \mathrm{X} 5 \mathrm{R}, 6.3 \mathrm{~V}$ | Murata | GRM185R60J105KE21 |
| 2 | RBO, RVCCO | Resistor, $2 \Omega$ | Vishay | CRCW06032R00F |
| 2 | RGCS1, RGCS2 | Resistor, $22.6 \mathrm{k} \Omega$ | Vishay | CRCW06032262F |
| 2 | RR1, RR2 | Resistor, $137 \mathrm{k} \Omega$ | Vishay | CRCW06031373F |
| 6 | $\begin{aligned} & \text { COV1, COV2, COV3, COV4, COV7, } \\ & \text { COV8 } \end{aligned}$ | OSCON, $560 \mu \mathrm{~F}, 2.5 \mathrm{~V}$ | Sanyo | 2SEPC560MZ |
| 4 | COV12, COV13, COV22, COV23 | MLCC, $47 \mu \mathrm{~F}, \mathrm{X} 5 \mathrm{R}$, 1206 | Murata | GRM31CR60J476ME19 |
| 2 | L1, L2 | Inductor, $0.47 \mu \mathrm{H}$ | Wurth Elektronik | 744355147 |
| 1 | RF12 | Resistor, $10 \mathrm{k} \Omega$ | Vishay | CRCW06031002F |
| 1 | RF11 | Resistor, $8.25 \mathrm{k} \Omega$ | Vishay | CRCW06038251F |
| 4 | QH1, QH2, QH3, QH4 | N MOSFET, $30 \mathrm{~V}, 9 \mathrm{~m} \Omega$ | Infineon | BSC080N03LS |
| 4 | QL1, QL2, QL3, QL4 | N MOSFET, $30 \mathrm{~V}, 4.5 \mathrm{~m} \Omega$ | Infineon | BSC030N03LS |
| 1 | CC11 | MLCC, 3300 pF | Vishay | VJ0603Y332KXAA |
| 1 | CC12 | MLCC, 180 pF | Vishay | VJ0603Y181KXAA |
| 1 | RC1 | Resistor, $8.87 \mathrm{k} \Omega$ | Vishay | CRCW06038871F |
| 2 | RLIM11, RLIM21 | Resistor, $1.74 \mathrm{k} \Omega$ | Vishay | CRCW06031741F |
| 2 | CLIM1, CLIM2 | MLCC, 22 pF | Vishay | VJ0603A220KXAA |
| 4 | J1, J2, J3, J4 | 3-terminal jumpers, 0.1 " spacing |  |  |
| 9 | R103, RT11, RT21, RDH1, RDH2, RDL1, RDL2, R1, R2 | Resistor, $0 \Omega$ | Vishay | CRCW06030R00F |
| 4 | T8, T9, T10, 111 | Test points, turret, 110-mil through hole | Keystone Electronics Corp. | 1502-1 |
| 4 | T1, T2, T5, T6 | Terminals, 20 A rated | Keystone Electronics Corp. | 8191 |

## Legal Terms and Conditions





















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