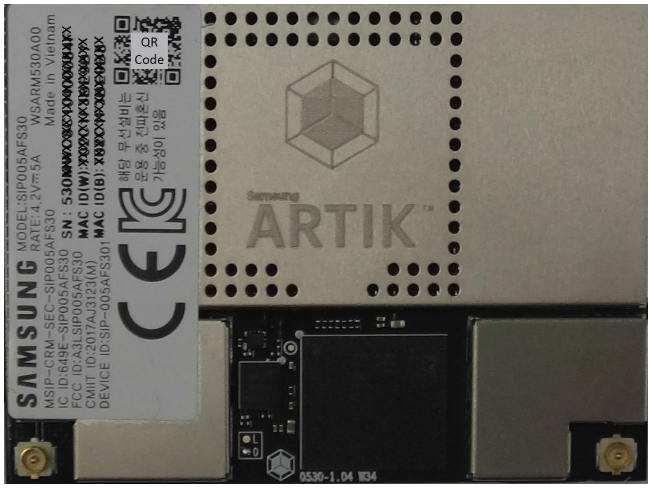
SAMSUNG

ARTIK™ Modules 5

ARTIK 530/530s Module Datasheet

1 Module Overview

ARTIK 530



ARTIK 530s and ARTIK 530s 1G

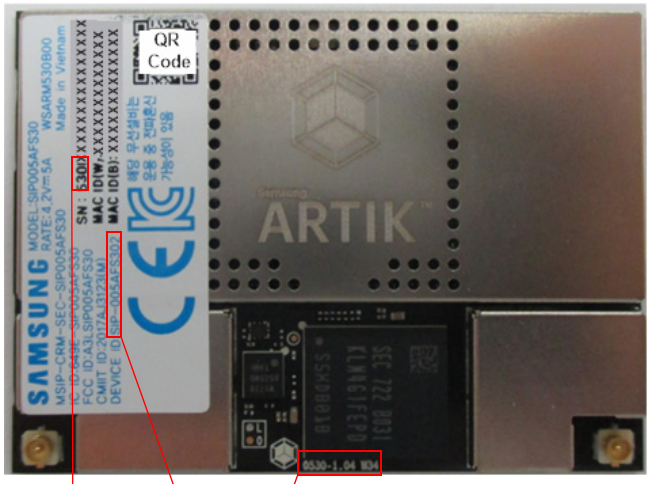


Figure 1. ARTIK™ 530/530s Module Top View

The Samsung ARTIK™ 530/530s Module is a highly-integrated System-in-Module that combines a quad-core ARM® Cortex®-A9 processor packaged with 512MB or 1GB DRAM and Flash memory, a Security Subsystem, and a wide range of wireless communication options—such as 802.11a/b/g/n for Wi-Fi®, Bluetooth® 4.2 (BLE+Classic), and 802.15.4 for Zigbee—all into one 49×36mm footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module's capabilities. With the combination of 802.11, Bluetooth, and 802.15.4, the ARTIK 530/530s Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element provides end-to-end security.

Processor	
CPU	Quad-core ARM® Cortex®-A9@1.2GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-lane MIPI CSI up to 5M (1920x1080@30fps)
Display	4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280×720p@60fps)
Audio	Two I^2S audio interfaces
Memory	
DRAM	512MB or 1GB DDR3 @ 800MHz
FLASH	4GB eMMC v4.5
Security	
Secure Element	Secure point-to-point authentication and data transfer
Trusted Execution Environment	Trustware
Radio	
WLAN	IEEE 802.11a/b/g/n, dual-band SISO
Bluetooth	4.2 (Classic+BLE)
LR_WPAN	IEEE 802.15.4
Power Management	
PMIC	Provides all power of the ARTIK 530/530s Module using onboard bucks and LDOs
Interfaces	
Ethernet	10/100/1000Base-T MAC (External PHY required)
Analog and Digital I/O	GPIO, UART, I^2C, SPI, SDIO, USB OTG, USB Host/ HSIC, ADC, PWM, I^2S, JTAG

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2 Version History

Revision	Date	Description
V1.0	January 20, 2017	First release.
V1.01	February 07, 2017	Updated Module PAD's section. Updated look and feel.
V1.02	April 12, 2017	Updated default behavior of GPIO pins to latest software release. Updated Booting Sequence section. 802.15.4 RF Specifications section. Updated Tables 1–36. Updated SD/MMC AC Electrical Characteristics section. Updated Recommended Operating Conditions section. Updated ESD section. Updated Power management section.
V1.03	November 20, 2017	In *Table 1*, definition of PU/PD and I/O columns for ballout and signal-description tables more explicitly defined. Characteristics for LDO3 (VCC3P3_SYS) removed, as using the output to drive external ICs is highly discouraged. Descriptions of other LDOs was removed, as they are not available externally. In *Functional Interfaces*, each subsection describing an interface that has alternate functions clarifies which are selected by hardware at power-on reset. Cross references added to the appropriate tables in *GPIO Alternate Functions*. Changed format of default functions in tables of *GPIO Alternate Functions* to make it easier to see which function number is the default. *Booting Selection* section rewritten for clarity. Power Sequence section divided into *Power Sequence* and *Power States*. Simplified power management state diagram, *Figure 5*. *Power/Current Consumption* section added.
V1.04	November 30,2017	Added ARTIK 530s and ARTIK 530s 1G features in *Module Overview*, *Block Diagram and Module Features*, and *Security Subsystem*. Caution after block diagram in *Block Diagram and Module Features* about not applying power before connecting antennas was deemed unnecessary and removed.
V1.05	November 30,2017	*Ordering Information*: Added ordering part numbers for ARTIK 530s 1G and its associated development kit.
V1.06	December 20, 2017	USB HOST/USB OTG: Changed function description of AP_OTG_ID signal. HSIC: Changed function descriptions for balls PAK12–14 and PAL12–14. *Mechanical Specifications*: Changed ball names in *Figure 13* and *Table 60* to correlate with ball organization shown in *Figure 3*. Note that the changes address a labeling consistency issue only; no electrical or layout changes are required.
V1.07	February 2, 2018	*CE*: Radio Equipment Directive (RED) certification update.
V1.08	April 5, 2018	*I^2C*: Removed support for slave mode. *Table 3*, *Table 9*: Marked pad PAL15 for internal use only. *Table 30*: Removed pad PAL15 from GPIO function table because it is reserved for internal use. Added *Temperature Thresholds for Operating Frequency Throttling* under new section *Thermal and Environmental Specifications*.
V1.09	May 29, 2018	*Figure 2*: Changed functional blocks for USB and HSIC. Changed *HSIC* to be a subheading to *USB HOST* to reflect hardware hierarchy. In *Functional Interfaces*, split USB OTG from USB Host and combined USB Host with HSIC. *Table 60*: Corrected X-locations of center pads. *Recommended Operating ConditionsRecommended Operating Conditions*: Added footnote about reduced retention time for Flash stored for an extended period of time at temperatures about 30°C. *Legal Information*: Clarified policy regarding third-party registered trademarks. General: Changed headings to a numbered format.
V1.10	June 25, 2018	*Figure 3*: Missing ball column 20 inserted..

3 Block Diagram and Module Features

Figure 2 shows the functional block diagram of the ARTIK 530/530s Module. It consists of a quad-core ARM® Cortex®-A9 application processor with 512MB or 1GB of DDR3 and 4GB eMMC Flash, PMIC power management, Security Subsystem, 802.11 for Wi-Fi®, Bluetooth®, 802.15.4 for Zigbee, and RF connectors.

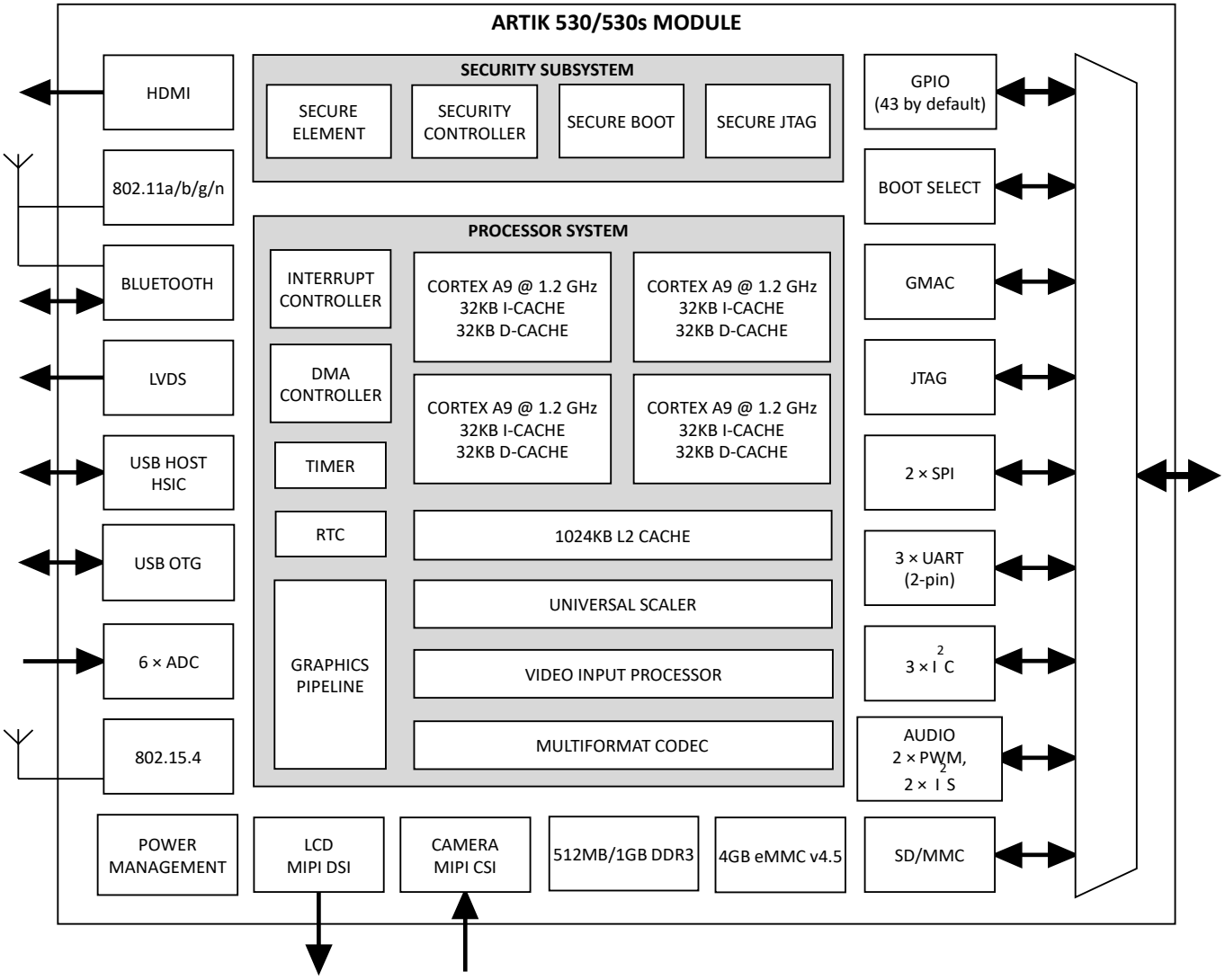

Figure 2. ARTIK 530/530s Module Functional Block Diagram

3.1 ARTIK 530/530s Module Features

The following subsections describe the functions of the various ARTIK 530/530s Module blocks depicted in *Figure 2*.

3.1.1 Quad-Core Processor System

The processor system architecture that resides on the ARTIK 530/530s Module is a system-on-a-chip (SoC) based on a 32-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using a quad-core CPU. The key features of the ARTIK 530/530s Module are

- Quad-core ARM® Cortex®-A9, 32-bit RISC architecture
- Maximum core speed 1.2GHz
- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between four cores
- Support for dynamic virtual-address mapping

3.1.2 Memory Controller

The ARTIK 530/530s Module has one DDR3 memory interface. The key features are

- One 32-bit DDR3 memory interface
- Two 256MB or two 512MB DDR3 16-bit memory chips, for a total of 512MB or 1GB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

3.1.3 Power Management

The ARTIK 530/530s Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has four fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%.The regulators operate at a fixed high frequency, minimizing noise in sensitive applications and allowing the use of small form factor components. These four regulators fully satisfy the power and control requirements of the ARTIK 530/530s Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I^2C control.

3.1.4 Wi-Fi

The ARTIK 530/530s Module has a fully integrated WLAN block covering IEEE 802.11 a/b/g/n. The most important hardware features of the module are

- 802.11 a/b/g/n dual-band SISO that is 2.4GHz/5GHz-compliant
- 1T1R 2.4GHz/5GHz band
- Support for 20MHzand 40MHz bandwidth (72.2/150Mbps PHY rate)
- Enhanced 802.11/Bluetooth coexistence control to improve transmission quality in different profiles
- Use of an SDIO interface

3.1.5 Bluetooth®

The ARTIK 530/530s Module has a fully integrated 4.2 block (BLE+Classic). The most important hardware features of the module are

- Bluetooth 4.2 (BLE+Classic)
- Enhanced 802.11/Bluetooth Coexistence control to improve transmission quality in different profiles

3.1.6 802.15.4 for Zigbee

The ARTIK 530/530s Module carries fully-integrated 802.15.4 functionality. The most important hardware features are

- Fully integrated 2.4 GHz, IEEE 802.15.4-compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M4 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.

3.1.7 USB OTG

The ARTIK 530/530s Module provides one USB 2.0 OTG interface supporting both device and host functionality. The key features of the USB 2.0 OTG sub-system are

- Compliant with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- High-speed (480Mbps) mode
- Full-speed (12Mbps) mode
- Low-speed (1.5Mbps) mode (host only)
- Support for session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- 16 host channels

3.1.8 USB HOST

The ARTIK 530/530s Module provides one USB 2.0 controller that is fully compliant with the USB 2.0 Host specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB 2.0 Host sub-system are

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices

- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support upstream/downstream port

3.1.8.1 HSIC

The ARTIK 530/530s Module provides one high-speed inter-chip (HSIC) version 1.0 module, controlled by the USB Host Controller. The key features of the HSIC sub-system are

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface
- Support for HSIC version 1.0

3.1.9 Gigabit EMAC

The ARTIK 530/530s Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6
- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

3.1.10 SD/MMC

The ARTIK 530/530s Module provides one SD/MMC interface. The Mobile Storage Host is an interface between the system and the SD/MMC. The key features of mobile storage host sub-system are as follows:

3.1.10.1 SD

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.10.2 MMC

- Support for Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.11 PCM

The ARTIK 530/530s Module provides one PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio . The key features of the PCM subsystem are

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2's complement, left justified, clock MSB first

3.1.12 MIPI CSI

The ARTIK 530/530s Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are

- 1, 2, 3 or 4 data lanes
- Support for the following image formats:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User-defined byte-based data packet
  - Compatible to PPI (Protocol to PHY interface)

3.1.13 MIPI DSI

The ARTIK 530/530s Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are

- Maximum resolution ranges up to WUXGA 1920 × 1200
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp
- Supported interfaces are
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Prescaler to generate escape clock from byte clock

3.1.14 HDMI

The ARTIK 530/530s Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

3.1.15 LVDS

The ARTIK 530/530s Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are

- Output clock range 30–125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

3.1.16 Video Input Processor

The ARTIK 530/530s Module provides one video input processor (VIP). The key features of the VIP sub-system are

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI-CSI
- Support for images up to 8192×8192
- Support for clipping and scale-down
- Support for YUV420 memory format

3.1.17 Scaler

The ARTIK 530/530s Module provides one universal scaler. The key features of the scaler are

- Support for different input formats:
  - YUV420, YUV422, YUV444
- Flexible size, from 8×8 up to 1920×1080 with a granularity of 8
- Upscale ratio from 8×8 to 1920×1080
- Downscale ratio from 1920×1080 to 8×8

- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

3.1.18 Multiformat Codec

The ARTIK 530/530s Module provides one integrated Multiformat Codec (MFC) module. The key features of the MFC sub-system are

- Decoder:
  - H.264 : BP, MP, HP Level 4.2 up to 1920×1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920×1080, at up to 40Mbps
  - H.263 : Profile 3 up to 1920×1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920×1080, up to 80MBps
- Encoder:
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

3.1.19 Graphics Pipeline

The ARTIK 530/530s Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are

- Two pixel processors:
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating-point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor:
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads

- Support for OpenGL ES 1.0 and 2.0

3.1.20 ADC

The ADC interface controls one 28nm low-power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are

- Up to six channels of analog input can be selected
- Conversion of analog input into 12-bit binary code up to 1 Mega Sample Per Second (MSPS)
- 1.0mW power consumption when running 1MSPS
- Input frequency up to 100kHz

3.1.21 GPIO

The ARTIK 530/530s Module provides a GPIO system with up to 107 GPIOs multiplexed with other I/O interface lines, as shown in *Figure 2* to support a wide variety of use-cases. The key features of the GPIO system are as follows:

- Both edge detect and level detect functionality
- Support for programmable pull-up/pull-down resistors
- Support for fast or normal slew operation
- Drive strength can be set from a register:

Value	Drive Strength *
0	2.6mA approximately (default)
1	5.2mA approximately
2	10.4mA approximately
3	15.6mA approximately

*. Assumes the reference I/O voltage is 3.3V. All drive-strength values are approximate. This value represents the current drive capability of GPIO pad only. Do not use GPIO as a current source.

- Support for interrupt generation that can be triggered on one of the following:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

3.1.22 I²S

The ARTIK 530/530s Module provides two 5-line Inter-IC Sound (I^2S) channels. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as subcoding and control. It is possible to transmit data between two I^2S buses. The key features of the I^2S sub-system are

- One-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Serial data transfer of 16/24 bits per channel in Master and Slave mode
- A variety of interface modes:
  - I^2S, Left justified, Right justified, DSP mode

3.1.23 Timer

The ARTIK 530/530s Module has four dedicated timer channels. The most important features of the Timer module are

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

3.1.23.1 PWM

The ARTIK 530/530s Module provides two pulse width modulation (PWM) instances with the following key features:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one-shot pulse mode
- Dead zone generator
- Level interrupt generation

3.1.24 SPI

The ARTIK 530/530s Module provides two Serial Peripheral Interface (SPI) portsthat transfer serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial Interface, National Semiconductor's Microwire, and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Compliant with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep

- Support for master mode and slave mode
- Support for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Supports Tx up to 50MHz, Rx up to 20MHz
  - Slave Mode : Supports Tx up to 8MHz, Rx up to 8MHz

3.1.25 UART

The ARTIK 530/530s Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are

- Separate 64×8 Tx and 64×8 Rx FIFO memory buffers
- Support for DMA-mode and interrupt-based mode of operation
- All independent channels support IrDA 1.0
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

3.1.26 I^2C

The ARTIK 530/530s Module provides three generic I^2C blocks supporting both 100kb/s and 400kb/s speed modes. The key features of the I^2C sub-system are

- Support for multi-master mode
- 7-bit addressing mode only
- Serial, 8-bit oriented and bi-directional data transfer
- Up to 100 kb/s in the standard mode
- Up to 400 kb/s in the fast mode
- Support for both interrupt and polling events

3.1.27 JTAG

The JTAG core provides debug capabilities for the developer and is compliant with the IEEE 1149 standard.

3.1.28 Interrupt Controller

The ARTIK 530/530s Module has one interrupt controller module. The most important features of the interrupt module are

- Vectored interrupt controller
- Support for 64 channel-interrupt sources

- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

3.1.29 DMA

The ARTIK 530/530s Module has one scatter-gather DMA module. The most important features of the DMA module are

- 16 channels of dedicated DMA
- 16 DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory-to-memory transfer
  - Memory-to-peripheral transfer
  - Peripheral-to-memory transfer
  - Peripheral-to-peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

3.1.30 RTC

The ARTIK 530/530s Module has one real time clock (RTC) module. The most important features are

- Four spread-spectrum PLLs
- Two external crystals: one 24MHz crystal for the PLLs and one 32.768KHz crystal for the RTC
- One 32-bit RTC counter
- Support for alarm interrupt using RTC
  -

3.1.31 Security Subsystem

In addition to the Secure Element, the main processor on the module provides additional security features. The key features of the Security Controller sub-system are

- Secure 128-bit die ID (available to the ARTIK 530s Modules only)

- Secure JTAG featuring a secure 128-bit JTAG ID (available to the ARTIK 530s Modules only)
- Secure boot featuring a 128-bit boot ID (available to the ARTIK 530s Modules only)
- Security Controller (available to the ARTIK 530s Modules only)
- Secure Element (all features in ARTIK 530s Modules; limited features in ARTIK 530 Module)

3.1.31.1 Security Controller

The Security Controller provides a Trusted Execution Environment (TEE) and hardware cryptographic accelerators as follows:

- TEE
  - Register Protection Controller
  - Memory Protection Controller
- Hardware cryptographic accelerators
  - DES, Triple DES
  - AES
  - SHA-1
  - MD5

3.1.31.2 Secure Element

The ARTIK 530/530s Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are

- An ISO/IEC 7816 14443-compliant interface.
- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read-only and 256B nonerasable Flash area
  - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
  - 32KB ROM
  - 264KB Flash
  - 2.5KB cryptographic memory
- Serial interfaces:
  - ISO 7816-3-compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

4 Module Pads

The ARTIK 530/530s Module utilizes 292 signal and ground balls providing all the relevant signaling. *Figure 3* shows how the balls are oriented and how signal coordinates are assigned to the PADs of the ARTIK 530/530s Module. *Table 2*–*Table 6* describe the relation between the ball coordinates and the ball signal names. These tables also provide detailed characteristics for each ball signal name.

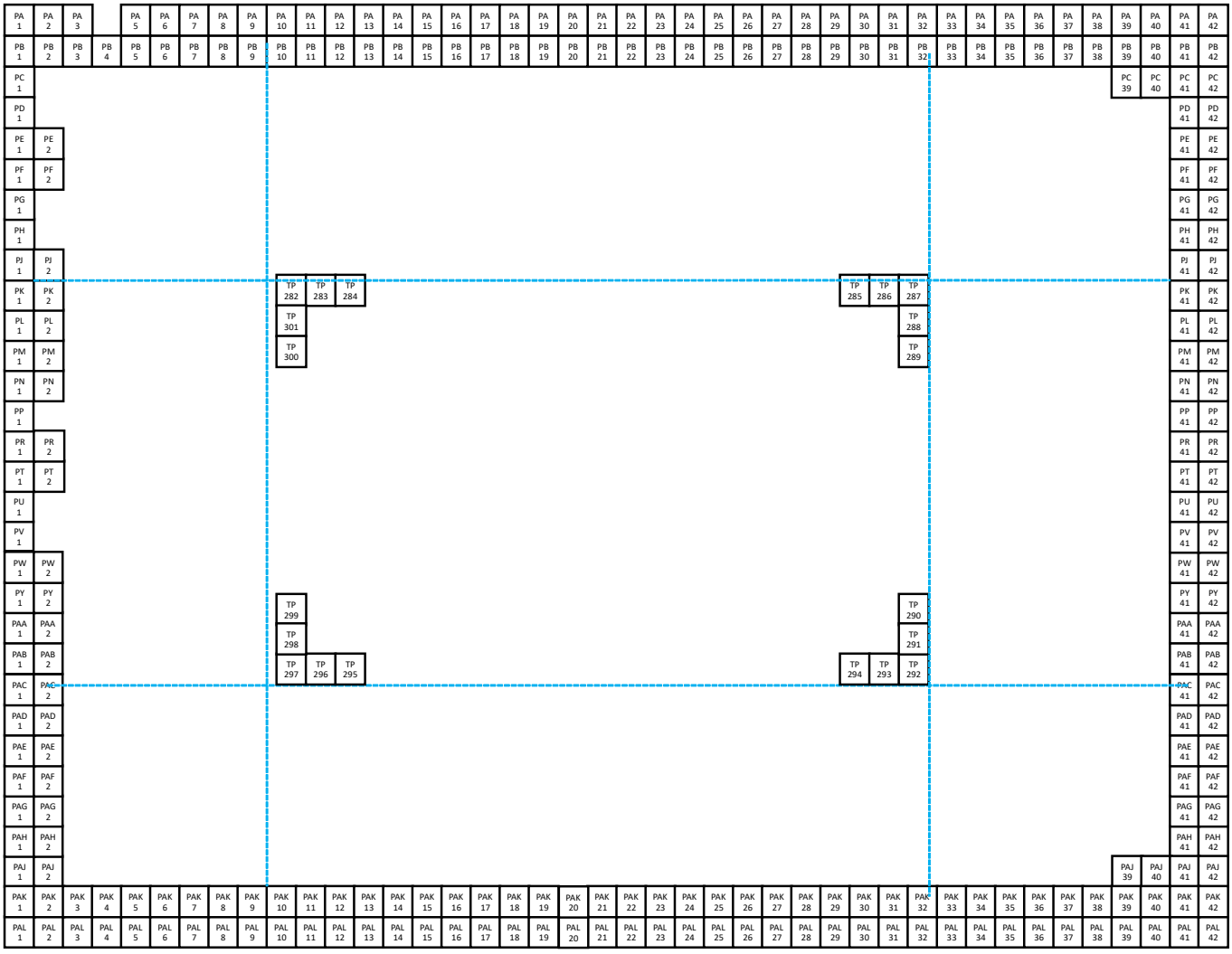

Figure 3. ARTIK 530/530s Module Top View Ball Organization

4.1 Ball Table Column Definitions

The meaning of the various columns used in *Table 2* - *Table 6* is explained in *Table 1*.

Table 1. Ball Table Column Definition

Column Name	Column Definition
Ball Loc.	Ball location on the ARTIK 530/530s Module as shown in *Figure 3*.
Ball Name	The ball name on the ARTIK 530/530s Module.
Voltage	Voltage level on the ball.
Default	Default function of the main SoC at hardware power-on.
Type	S: Signal ball, P: Power ball, G: GND ball.
I/O	I: Input, O: Output, IO: Input/Output to/from module
PU/PD	Indicates the presence of module-internal pull-up or pull-down. PU: Pull-Up, PD: Pull-Down, N: No Pull-Up/Pull-Down.
Group	Nominal function group set according to pad name. For more information see the ARTIK 530/530s Module Hardware User Guide. Usually the function of the pin can be reprogrammed.
Function	Explanation on the function of the ball.

4.1.1 North Ball Array

Table 2. North Ball Array

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PA1	GMAC_TXEN	3.3V	S	IO	N	GMAC	GMAC Transmit Enable
PA2	GMAC_TXD1	3.3V	S	IO	N	GMAC	GMAC Transmit Data 1
PA3	GMAC_TXD3	3.3V	S	IO	N	GMAC	GMAC Transmit Data 3
PA4	NO BALL	–	–	–	–	NO BALL	–
PA5	GMAC_GTXCLK	3.3V	S	IO	N	GMAC	GMAC Transmit Clock
PA6	GMAC_RXDV	3.3V	S	IO	N	GMAC	GMAC Receive Enable
PA7	GMAC_RXD2	3.3V	S	IO	N	GMAC	GMAC Receive Data 2
PA8	GMAC_RXD0	3.3V	S	IO	N	GMAC	GMAC Receive Data 0
PA9	GND	0.0V	G	–	–	GND	Ground
PA10	AP_MIPICSI_DNCLK	1.8V	S	IO	N	CSI	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 3
PA15	GND	0.0V	G	–	–	GND	Ground
PA16	AP_MIPIDSI_DNCLK	1.8V	S	IO	N	DSI	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 3
PA21	GND	0.0V	G	–	–	GND	Ground
PA22	AP_LVDS_TN0	1.8V	S	O	N	LVDS	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1.8V	S	O	N	LVDS	LVDS Transmit Channel 1 Negative

Table 2. North Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PA24	AP_LVDS_TN2	1.8V	S	O	N	LVDS	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1.8V	S	O	N	LVDS	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1.8V	S	O	N	LVDS	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1.8V	S	O	N	LVDS	LVDS Transmit Channel 4 Negative
PA28	GND	0.0V	G	–	–	GND	Ground
PA29	AP_HDMI_CEC	3.3V	S	IO	N	HDMI	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1.8V	S	O	N	HDMI	HDMI Transmit Channel 2 Negative
PA31	AP_HDMI_TX1N	1.8V	S	O	N	HDMI	HDMI Transmit Channel 1 Negative
PA32	AP_HDMI_TX0N	1.8V	S	O	N	HDMI	HDMI Transmit Channel0 Negative
PA33	AP_HDMI_TXCN	1.8V	S	O	N	HDMI	HDMI Transmit Negative Clock
PA34	GND	0.0V	G	–	–	GND	Ground
PA35	AP_OTG_DM	3.3V	S	IO	N	USB OTG	USB OTG Data Minus
PA36	AP_USBH_DM	3.3V	S	IO	N	USB HOST	USB HOST Data Minus
PA37	AP_GPA13	3.3V	S	IO	N	GPIO	Generic GPIO
PA38	AP_HSIC_STROBE	1.2V	S	IO	N	HSIC	HSIC Strobe
PA39	AP_GPA14	3.3V	S	IO	N	GPIO	Generic GPIO
PA40	AP_GPA9	3.3V	S	IO	N	GPIO	Generic GPIO
PA41	AP_GPA15	3.3V	S	IO	N	GPIO	Generic GPIO
PA42	AP_GPA12	3.3V	S	IO	N	GPIO	Generic GPIO
PB1	GND	0.0V	G	–	–	GND	Ground
PB2	GMAC_TXD0	3.3V	S	IO	N	GMAC	GMAC Transmit Data 0
PB3	GMAC_TXD2	3.3V	S	IO	N	GMAC	GMAC Transmit Data 2
PB4	GMAC_MDC	3.3V	S	IO	N	GMAC	GMAC MDC
PB5	GMAC_RXCLK	3.3V	S	IO	N	GMAC	GMAX Receive Clock
PB6	GMAC_RXD3	3.3V	S	IO	N	GMAC	GMAC Receive Data 3
PB7	GMAC_RXD1	3.3V	S	IO	N	GMAC	GMAC Receive Data 1
PB8	GMAC_MDIO	3.3V	S	IO	N	GMAC	GMAC MDIO
PB9	GND	0.0V	G	–	–	GND	Ground
PB10	AP_MIPICSI_DPCLK	1.8V	S	IO	N	CSI	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 3
PB15	GND	0.0V	G	–	–	GND	Ground
PB16	AP_MIPIDSI_DPCLK	1.8V	S	IO	N	DSI	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 3
PB21	GND	0.0V	G	–	–	GND	Ground
PB22	AP_LVDS_TP0	1.8V	S	O	N	LVDS	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1.8V	S	O	N	LVDS	LVDS Transmit Channel 1 Positive

Table 2. North Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PB24	AP_LVDS_TP2	1.8V	S	O	N	LVDS	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1.8V	S	O	N	LVDS	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1.8V	S	O	N	LVDS	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1.8V	S	O	N	LVDS	LVDS Transmit Channel 4 Positive
PB28	GND	0.0V	G	–	–	GND	Ground
PB29	AP_HDMI_HPD	3.3V	S	I	N	HDMI	HDMI Hot Plug Detect
PB30	AP_HDMI_TX2P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 2 Positive
PB31	AP_HDMI_TX1P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 1 Positive
PB32	AP_HDMI_TX0P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 0 Positive
PB33	AP_HDMI_TXCP	1.8V	S	O	N	HDMI	HDMI Transmit Positive Clock
PB34	GND	0.0V	G	–	–	GND	Ground
PB35	AP_OTG_DP	3.3V	S	IO	N	USB OTG	USB OTG Data Plus
PB36	AP_USBH_DP	3.3V	S	IO	N	USB HOST	USB HOST Data Plus
PB37	AP_OTG_ID	–	S	I	N	USB HOST	USB HOST ID
PB38	AP_HSIC_DATA	1.2V	S	IO	N	HSIC	HSIC Data
PB39	AP_GPA4	3.3V	S	IO	N	GPIO	Generic GPIO
PB40	AP_GPA5	3.3V	S	IO	N	GPIO	Generic GPIO
PB41	AP_GPA16	3.3V	S	IO	N	GPIO	Generic GPIO
PB42	AP_GPA11	3.3V	S	IO	N	GPIO	Generic GPIO

4.1.2 South Ball Array

Table 3. South Ball Array

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PAK1	AP_I2S0_DOUT	3.3V	S	IO	N	I2S0	I^2S 0 Data Out
PAK2	AP_I2S0_BCLK	3.3V	S	IO	N	I2S0	I^2S 0 Bit Clock
PAK3	AP_GPC11_SPI2_MISO	3.3V	S	IO	N	SPI2	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3.3V	S	IO	N	SPI2	SPI 2 Clock
PAK5	AP_SPI0_MISO	3.3V	S	IO	N	SPI0	SPI 0 Receive Data *
PAK6	AP_SPI0_CLK	3.3V	S	IO	N	SPI0	SPI 0 Clock *
PAK7	AP_GPC14_PWM2	3.3V	S	IO	N	PWM	PWM 2
PAK8	AP_GPD6_SCL2	3.3V	S	IO	PU	I^2C	I^2C SCL 2
PAK9	AP_GPD4_SCL1	3.3V	S	IO	PU	I^2C	I^2C SCL 1
PAK10	AP_GPD2_SCL0	3.3V	S	IO	PU	I^2C	I^2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3.3V	S	IO	N	I^2C	HDMI I^2C SCL *
PAK12	ZB_DEBUG_TDO_SWO	3.3V	–	–	–	802.15.4	802.15.4 JTAG TMS
PAK13	ZB_PTI_DATA_FRC_DOUT	3.3V	–	–	–	802.15.4	802.15.4 JTAG TCK
PAK14	ZB_DEBUG_TCK_SWCLK	3.3V	–	–	–	802.15.4	802.15.4 Control
PAK15	COMBO_ZIG_UART_TXD	3.3V	S	IO	–	802.15.4	802.15.4 UART
PAK16	GND	0.0V	G	–	–	GND	Ground

Table 3. South Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PAK17	VCC3P3_SYS	3.3V	P	O	–	POWER	VCC 3.3V Power: voltage reference only
PAK18	VCC3P3_SYS	3.3V	P	O	–	POWER	VCC 3.3V Power: voltage reference only
PAK19	AP_GPD28	3.3V	S	IO	N	GPIO	Generic GPIO
PAK20	AP_GPE2	3.3V	S	IO	N	GPIO	Generic GPIO
PAK21	AP_GPE1	3.3V	S	IO	N	GPIO	Generic GPIO
PAK22	AP_UARTTX3	3.3V	S	IO	N	UART	UART Transmit Data 3
PAK23	AP_UARTTX4	3.3V	S	IO	N	UART	UART Transmit Data 4
PAK24	AP_UARTTX0	3.3V	S	IO	N	UART	UART Transmit Data 0
PAK25	AP_GPB0_VID1_1_I2SLRCK1	3.3V	S	IO	PU	I2S1	I^2S 1 Left Right Clock *
PAK26	AP_GPA28_I2SMCLK1	3.3V	S	IO	N	I2S1	I^2S 1 Master Clock *
PAK27	AP_GPA30_VID1_0_I2SBCLK1	3.3V	S	IO	PU	I2S1	I^2S 1 Bit Clock *
PAK28	AP_SD0_CMD	3.3V	S	IO	N	SD/MMC	SD Command
PAK29	AP_SD0_D1	3.3V	S	IO	N	SD/MMC	SD Data 1
PAK30	AP_SD0_CLK	3.3V	S	IO	N	SD/MMC	SD Clock
PAK31	NO CONNECTION	–	–	–	–	NC	NA
PAK32	AP_GPB13_SD0_BOOT	3.3V	S	I	PU	BOOTING	Select Booting Scenario
PAK33	AP_GPC17	3.3V	S	IO	N	GPIO	Generic GPIO
PAK34	AP_GPC0	3.3V	S	IO	N	GPIO	Generic GPIO
PAK35	AP_GPC26	3.3V	S	IO	PU	GPIO	Generic GPIO
PAK36	AP_GPB8	3.3V	S	IO	N	GPIO	Generic GPIO
PAK37	AP_GPB14	3.3V	S	IO	N	GPIO	Generic GPIO
PAK38	AP_GPA20	3.3V	S	IO	N	GPIO	Generic GPIO
PAK39	AP_GPA18	3.3V	S	IO	N	GPIO	Generic GPIO
PAK40	AP_GPA21	3.3V	S	IO	N	GPIO	Generic GPIO
PAK41	AP_GPA10	3.3V	S	IO	N	GPIO	Generic GPIO
PAK42	AP_GPA6	3.3V	S	IO	N	GPIO	Generic GPIO
PAL1	AP_I2S0_DIN	3.3V	S	IO	N	I2S0	I^2S 0 Data In
PAL2	AP_I2S0_MCLK	3.3V	S	IO	N	I2S0	I^2S 0 Master Clock
PAL3	AP_GPC12_SPI2_MOSI	3.3V	S	IO	N	SPI2	SPI 2 Transmit Data
PAL4	AP_GPC10_SPI2_CS	3.3V	S	IO	PU	SPI2	SPI 2 Frame
PAL5	AP_SPI0_MOSI	3.3V	S	IO	N	SPI0	SPI 0 Transmit Data *
PAL6	AP_SPI0_CS	3.3V	S	IO	N	SPI0	SPI 0 Frame *
PAL7	AP_GPD1_PWM0	3.3V	S	IO	N	PWM	PWM 0
PAL8	AP_GPD7_SDA2	3.3V	S	IO	PU	I^2C	I^2C SDA 2
PAL9	AP_GPD5_SDA1	3.3V	S	IO	PU	I^2C	I^2C SDA 1
PAL10	AP_GPD3_SDA0	3.3V	S	IO	PU	I^2C	I^2C SDA 0
PAL11	AP_GPA24_HDMI_I2C_SDA	3.3V	S	IO	N	I^2C	HDMI I^2C SDA *
PAL12	ZB_DEBUG_TMS_SWDIO	3.3V	–	–	–	802.15.4	802.15.4 JTAG TDI
PAL13	ZB_PTI_SYNC_FRC_DFRAME	3.3V	–	–	–	802.15.4	802.15.4 JTAG TDO
PAL14	PAD_ZB_RSTn	3.3V	S	O	N	802.15.4	802.15.4 Reset
PAL15	COMBO_ZIG_UART_RXD	3.3V	S	IO	PU	802.15.4	802.15.4 UART (for internal use only)
PAL16	GND	0.0V	G	–	–	GND	Ground

Table 3. South Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PAL17	VCC3P3_SYS	3.3V	P	O	–	POWER	VCC 3V3 Power: voltage reference only
PAL18	VCC3P3_SYS	3.3V	P	O	–	POWER	VCC 3V3 Power: voltage reference only
PAL19	AP_VDDPWRON	3.3V	S	O	N	MISC	VDD Power On
PAL20	AP_GPE3	3.3V	S	IO	N	GPIO	Generic GPIO
PAL21	AP_GPE0	3.3V	S	IO	N	GPIO	Generic GPIO
PAL22	AP_UART_RX3	3.3V	S	IO	N	UART	UART Receive Data 3
PAL23	AP_UART_RX4	3.3V	S	IO	N	UART	UART Receive Data 4
PAL24	AP_UART_RX0	3.3V	S	IO	N	UART	UART Receive Data 0
PAL25	AP_GPD31	3.3V	S	IO	N	GPIO	Generic GPIO
PAL26	AP_GPB9_I2SDIN1	3.3V	S	IO	N	I2S1	I^2S 1 Data In *
PAL27	AP_GPB6_VID1_4_I2SDOUT1	3.3V	S	IO	PD	I2S1	I^2S 1 Data Out *
PAL28	AP_SD0_D3	3.3V	S	IO	N	SD/MMC	SD Data 3
PAL29	AP_SD0_D2	3.3V	S	IO	N	SD/MMC	SD Data 2
PAL30	AP_SD0_D0	3.3V	S	IO	N	SD/MMC	SD Data 0
PAL31	AP_GPB4_VID1_3_BOOT	3.3V	S	I	PU	BOOTING	Select Booting Scenario
PAL32	AP_GPB15_SD1_BOOT	3.3V	S	I	PD	BOOTING	Select Booting Scenario
PAL33	AP_GPD8	3.3V	S	IO	N	GPIO	Generic GPIO
PAL34	AP_GPE30	3.3V	S	IO	PU	GPIO	Generic GPIO
PAL35	AP_GPC27	3.3V	S	IO	PU	GPIO	Generic GPIO
PAL36	AP_GPB22	3.3V	S	IO	N	GPIO	Generic GPIO
PAL37	AP_GPB16	3.3V	S	IO	N	GPIO	Generic GPIO
PAL38	AP_GPB23	3.3V	S	IO	N	GPIO	Generic GPIO
PAL39	AP_GPA22	3.3V	S	IO	N	GPIO	Generic GPIO
PAL40	AP_GPA19	3.3V	S	IO	N	GPIO	Generic GPIO
PAL41	AP_GPA17	3.3V	S	IO	N	GPIO	Generic GPIO
PAL42	AP_GPA3	3.3V	S	IO	N	GPIO	Generic GPIO

*. Functions as general-purpose GPIO by default

4.1.3 East Ball Array

Table 4. East Ball Array

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PC1	GND	0.0V	G	–	–	GND	Ground
PC2	NO BALL	–	–	–	–	NO BALL	–
PD1	GND	0.0V	G	–	–	GND	Ground
PD2	NO BALL	–	–	–	–	NO BALL	–
PE1	GND	0.0V	G	–	–	GND	Ground
PE2	GND	0.0V	G	–	–	GND	Ground
PF1	GND	0.0V	G	–	–	GND	Ground
PF2	GND	0.0V	G	–	–	GND	Ground
PG1	GND	0.0V	G	–	–	GND	Ground

Table 4. East Ball Array (Continued)

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PG2	NO BALL	–	–	–	–	NO BALL	–
PH1	GND	0.0V	G	–	–	GND	Ground
PH2	NO BALL	–	–	–	–	NO BALL	–
PJ1	GND	0.0V	G	–	–	GND	Ground
PJ2	GND	0.0V	G	–	–	GND	Ground
PK1	GND	0.0V	G	–	–	GND	Ground
PK2	GND	0.0V	G	–	–	GND	Ground
PL1	GND	0.0V	G	–	–	GND	Ground
PL2	GND	0.0V	G	–	–	GND	Ground
PM1	GND	0.0V	G	–	–	GND	Ground
PM2	GND	0.0V	G	–	–	GND	Ground
PN1	GND	0.0V	G	–	–	GND	Ground
PN2	GND	0.0V	G	–	–	GND	Ground
PP1	GND	0.0V	G	–	–	GND	Ground
PP2	NO BALL	–	–	–	–	NO BALL	–
PR1	GND	0.0V	G	–	–	GND	Ground
PR2	GND	0.0V	G	–	–	GND	Ground
PT1	GND	0.0V	G	–	–	GND	Ground
PT2	GND	0.0V	G	–	–	GND	Ground
PU1	GND	0.0V	G	–	–	GND	Ground
PU2	NO BALL	–	–	–	–	NO BALL	–
PV1	GND	0.0V	G	–	–	GND	Ground
PV2	NO BALL	–	–	–	–	NO BALL	–
PW1	AP_ADC4	1.8V	S	I	N	ADC	ADC Channel 4
PW2	AP_ADC5	1.8V	S	I	N	ADC	ADC Channel 5
PY1	AP_ADC0	1.8V	S	I	N	ADC	ADC Channel 0
PY2	AP_ADC1	1.8V	S	I	N	ADC	ADC Channel 1
PAA1	AP_ADC2	1.8V	S	I	N	ADC	ADC Channel 2
PAA2	AP_ADC3	1.8V	S	I	N	ADC	ADC Channel 3
PAB1	GND	0.0V	G	–	–	GND	Ground
PAB2	GND	0.0V	G	–	–	GND	Ground
PAC1	AP_TCK	3.3V	S	IO	PD	JTAG	JTAG TCK
PAC2	AP_TMS	3.3V	S	IO	PU	JTAG	JTAG TMS
PAD1	AP_TDO	3.3V	S	IO	N	JTAG	JTAG TDO
PAD2	AP_TDI	3.3V	S	IO	PU	JTAG	JTAG TDI
PAE1	AP_NTRST	3.3V	S	IO	PU	JTAG	JTAG NTRST
PAE2	AP_AGP2_RTC_INT_N	3.3V	S	IO	N	KEY/ ALIVE	AliveGPIO
PAF1	AP_PWRKEY	3.3V	S	IO	N	KEY/ ALIVE	Power Key part of AliveGPIO
PAF2	AP_AGP1	3.3V	S	IO	N	ALIVE	AliveGPIO
PAG1	AP_NRESET	3.3V	S	I	N *	KEY	Reset
PAG2	AP_GPA25	3.3V	S	IO	N	GPIO	Generic GPIO

Table 4. East Ball Array (Continued)

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PAH1	AP_GPA26	3.3V	S	IO	N	GPIO	Generic GPIO
PAH2	AP_GPA0	3.3V	S	IO	N	GPIO	Generic GPIO
PAJ1	AP_I2S0_LRCLK	3.3V	S	IO	N	I2S0	I^2S 0 Left Right Clock
PAJ2	AP_GPA27	3.3V	S	IO	N	I2S0	Generic GPIO

*. External 100kΩ pull-up resistor required.

4.1.4 West Ball Array

Table 5. West Ball Array

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PC39	GND	0.0V	G	–	–	GND	Ground
PC40	GND	0.0V	G	–	–	GND	Ground
PC41	GND	0.0V	G	–	–	GND	Ground
PC42	GND	0.0V	G	–	–	GND	Ground
PD41	VCC5P0_OTGVBUS	–	P	I	–	POWER	USB2.0 OTG BUS Power
PD42	VCC5P0_OTGVBUS	–	P	I	–	POWER	USB 2.0 OTG BUS Power
PE41	NO CONNECTION	–	–	–	–	NC	–
PE42	NO CONNECTION	–	–	–	–	NC	–
PF41	NO CONNECTION	–	–	–	–	NC	–
PF42	GND	0.0V	G	–	–	GND	Ground
PG41	GND	0.0V	G	–	–	GND	Ground
PG42	GND	0.0V	G	–	–	GND	Ground
PH41	NO CONNECTION	–	–	–	–	NC	–
PH42	NO CONNECTION	–	–	–	–	NC	–
PJ41	NO CONNECTION	–	–	–	–	NC	–
PJ42	GND	0.0V	G	–	–	GND	Ground
PK41	GND	0.0V	G	–	–	GND	Ground
PK42	GND	0.0V	G	–	–	GND	Ground
PL41	GND	0.0V	G	–	–	GND	Ground
PL42	GND	0.0V	G	–	–	GND	Ground
PM41	GND	0.0V	G	–	–	GND	Ground
PM42	GND	0.0V	G	–	–	GND	Ground
PN41	GND	0.0V	G	–	–	GND	Ground
PN42	GND	0.0V	G	–	–	GND	Ground
PP41	AP_GPB30	3.3V	S	IO	–	GPIO	Generic GPIO
PP42	GND	0.0V	G	–	–	GND	Ground
PR41	NO CONNECTION	–	–	–	–	NC	–
PR42	NO CONNECTION	–	–	–	–	NC	–
PT41	GND	0.0V	G	–	–	GND	Ground
PT42	GND	0.0V	G	–	–	GND	Ground
PU41	GND	0.0V	G	–	–	GND	Ground

Table 5. West Ball Array (Continued)

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PU42	GND	0.0V	G	–	–	GND	Ground
PV41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PV41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PW41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PW42	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PY41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PY42	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PAA41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PAA42	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PAB41	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PAB42	VIN	3.7~5.0V	P	I	–	POWER	Main Power Supply for Module
PAC41	GND	0.0V	G	–	–	GND	Ground
PAC42	GND	0.0V	G	–	–	GND	Ground
PAD41	NO CONNECTION	–	–	–	–	NC	–
PAD42	NO CONNECTION	–	–	–	–	NC	–
PAE41	GND	0.0V	G	–	–	GND	Ground
PAE42	NO CONNECTION	–	–	–	–	NC	–
PAF41	GND	0.0V	G	–	–	GND	Ground
PAF42	GND	0.0V	G	–	–	GND	Ground
PAG41	AP_GPB11	3.3V	S	IO	N	GPIO	Generic GPIO
PAG42	AP_GPB18	3.3V	S	IO	N	GPIO	Generic GPIO
PAH41	AP_GPC25	3.3V	S	IO	PU	GPIO	Generic GPIO
PAH42	AP_GPE31	3.3V	S	IO	PU	GPIO	Generic GPIO
PAJ39	BT_PCM_CLK	3.3V	S	IO	N	BT PCM	PCM Clock
PAJ40	BT_PCM_D_IN	3.3V	S	I	N	BT PCM	PCM Data In
PAJ41	BT_PCM_D_OUT	3.3V	S	O	N	BT PCM	PCM Data Out
PAJ42	BT_PCM_LRCK	3.3V	S	IO	N	BT PCM	PCM LR Clock

4.1.5 Center Ball Array

Table 6. Center Ball Array

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
TP282	GND	0.0V	NA	–	–	GND	Ground
TP283	GND	0.0V	NA	–	–	GND	Ground
TP284	GND	0.0V	NA	–	–	GND	Ground
TP285	GND	0.0V	NA	–	–	GND	Ground
TP286	GND	0.0V	NA	–	–	GND	Ground
TP287	GND	0.0V	NA	–	–	GND	Ground
TP288	GND	0.0V	NA	–	–	GND	Ground
TP289	GND	0.0V	NA	–	–	GND	Ground
TP290	GND	0.0V	NA	–	–	GND	Ground
TP291	GND	0.0V	NA	–	–	GND	Ground

Table 6. Center Ball Array (Continued)

Ball	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
TP292	GND	0.0V	NA	–	–	GND	Ground
TP293	GND	0.0V	NA	–	–	GND	Ground
TP294	GND	0.0V	NA	–	–	GND	Ground
TP295	GND	0.0V	NA	–	–	GND	Ground
TP296	GND	0.0V	NA	–	–	GND	Ground
TP297	GND	0.0V	NA	–	–	GND	Ground
TP298	GND	0.0V	NA	–	–	GND	Ground
TP299	GND	0.0V	NA	–	–	GND	Ground
TP300	GND	0.0V	NA	–	–	GND	Ground
TP301	GND	0.0V	NA	–	–	GND	Ground

5 Functional Interfaces

This section shows the functional interfaces that are available at the pads of the ARTIK 530/530s Module. The functions provided are related to the development environment used. Depending on your project you can always choose to reprogram some of the GPIOs that are currently assigned to the predefined functional interfaces.

5.1 Power

Table 7. Power

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
3.3V System Power	PAK[17,18] PAL[17,18]	VCC3P3_SYS*	3.3V	O	–
USB 2.0 OTG Bus Power	PD[41,42]	VCC5P0_OTGVBUS	5.0V	I	–
Main Power Supply for Module	PV[41,42] PW[41,42] PY[41,42] PAA[41,42] PAB[41,42]	VIN	3.7–5.0V	I	–

*. VCC3P3_SYS pads are not recommended as a current source; do not use them to drive external ICs. VCC3P3_SYS pads turn off when the ARTIK 530/530s Module goes into sleep mode.

5.2 AliveGPIO

Table 8. Key

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
AliveGPIO 1	PAF2	AP_AGP1	3.3V	IO	N
AliveGPIO 2	PAE2	AP_AGP2_RTC_INT_N	3.3V	IO	N
Power Key part of AliveGPIO	PAF1	AP_PWRKEY	3.3V	IO	N
Reset	PAG1	AP_NRESET	3.3V	I	N *

*. External 100kΩ pull-up resistor required.

5.3 802.15.4 for Zigbee

Table 9. 802.15.4

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
802.15.4 JTAG Test Clock	PAK14	ZB_DEBUG_TCK_SWCLK	3.3V	–	–
802.15.4 Frame Control	PAK13	ZB_PTI_DATA_FRC_DOUT	3.3V	–	–
802.15.4 Debug Serial Wire I/O & Test Mode Select	PAL12	ZB_DEBUG_TMS_SWDIO	3.3V	–	–
802.15.4 Debug Serial Wire Viewer Out	PAL13	ZB_PTI_SYNC_FRC_DFRAME	3.3V	–	–
802.15.4 JTAG Test Data Out	PAK12	ZB_DEBUG_TDO_SWO	3.3V	–	–
802.15.4 Reset	PAL14	PAD_ZB_RSTn	3.3V	O	N

Table 9. 802.15.4 (Continued)

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
802.15.4 UART	PAK15	COMBO_ZIG_UART_TXD	3.3V	IO	–
802.15.4 UART *	PAL15	COMBO_ZIG_UART_RXD	3.3V	IO	PU

*. For internal use only.

5.4 USB OTG

Table 10. USB OTG

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
USB OTG ID	PB37	AP_OTG_ID	1.8V	I	N
USB OTG Data Minus	PA35	AP_OTG_DM	3.3V	IO	N
USB OTG Data Plus	PB35	AP_OTG_DP	3.3V	IO	N

5.5 USB HOST/HSIC

Table 11. USB Host

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
USB Host Data Minus	PA36	AP_USBH_DM	3.3V	IO	N
USB Host Data Plus	PB36	AP_USBH_DP	3.3V	IO	N
HSIC Data	PB38	AP_HSIC_DATA	1.2V	IO	N
HSIC Strobe	PA38	AP_HSIC_STROBE	1.2V	IO	N

5.6 GMAC

The GMAC interface is available if GPIO alternate function 1 is selected on each pad.

Table 12. GMAC

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
GMAC MDC	PB4	GMAC_MDC	3.3V	IO	N
GMAC MDIO	PB8	GMAC_MDIO	3.3V	IO	N
GMAC Receive Clock	PB5	GMAC_RXCLK	3.3V	IO	N
GMAC Receive Data 0	PA8	GMAC_RXD0	3.3V	IO	N
GMAC Receive Data 1	PB7	GMAC_RXD1	3.3V	IO	N
GMAC Receive Data 2	PA7	GMAC_RXD2	3.3V	IO	N
GMAC Receive Data 3	PB6	GMAC_RXD3	3.3V	IO	N
GMAC Receive Enable	PA6	GMAC_RXDV	3.3V	IO	N
GMAC Transmit Clock	PA5	GMAC_GTXCLK	3.3V	IO	N
GMAC Transmit Data 0	PB2	GMAC_TXD0	3.3V	IO	N
GMAC Transmit Data 1	PA2	GMAC_TXD1	3V3	IO	N
GMAC Transmit Data 2	PB3	GMAC_TXD2	3.3V	IO	N

Table 12. GMAC (Continued)

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
GMAC Transmit Data 3	PA3	GMAC_TXD3	3.3V	IO	N
GMAC Transmit Enable	PA1	GMAC_TXEN	3.3V	IO	N

The above signals can be reassigned by software to alternate functions; see *Table 29* for details.

5.7 SD/MMC

Table 13. SD/MMC

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
SD Clock	PAK30	AP_SD0_CLK	3.3V	IO	N
SD Command	PAK28	AP_SD0_CMD	3.3V	IO	N
SD Data 0	PAL30	AP_SD0_D0	3.3V	IO	N
SD Data 1	PAK29	AP_SD0_D1	3.3V	IO	N
SD Data 2	PAL29	AP_SD0_D2	3.3V	IO	N
SD Data 3	PAL28	AP_SD0_D3	3.3V	IO	N

The above signals can be reassigned by software to alternate functions; see *Table 30* for details.

5.8 Bluetooth PCM

Table 14. Bluetooth PCM

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
PCM Clock	PAJ39	BT_PCM_CLK	3.3V	IO	N
PCM LR Clock	PAJ42	BT_PCM_LRCK	3.3V	IO	N
PCM Data In	PAJ40	BT_PCM_D_IN	3.3V	I	N
PCM Data Out	PAJ41	BT_PCM_D_OUT	3.3V	O	N

5.9 MIPI CSI

Table 15. MIPI CSI

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
MIPI CSI Data Negative Clock	PA10	AP_MIPICSI_DNCLK	1.8V	IO	N
MIPI CSI Data Negative 0	PA11	AP_MIPICSI_DN0	1.8V	IO	N
MIPI CSI Data Negative 1	PA12	AP_MIPICSI_DN1	1.8V	IO	N
MIPI CSI Data Negative 2	PA13	AP_MIPICSI_DN2	1.8V	IO	N
MIPI CSI Data Negative 3	PA14	AP_MIPICSI_DN3	1.8V	IO	N
MIPI CSI Data Positive Clock	PB10	AP_MIPICSI_DPCLK	1.8V	IO	N
MIPI CSI Data Positive 0	PB11	AP_MIPICSI_DP0	1.8V	IO	N

Table 15. MIPI CSI (Continued)

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
MIPI CSI Data Positive 1	PB12	AP_MIPICSI_DP1	1.8V	IO	N
MIPI CSI Data Positive 2	PB13	AP_MIPICSI_DP2	1.8V	IO	N
MIPI CSI Data Positive 3	PB14	AP_MIPICSI_DP3	1.8V	IO	N

5.10 MIPI DSI

Table 16. MIPI DSI

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
MIPI DSI Data Negative Clock	PA16	AP_MIPIDSI_DNCLK	1.8V	IO	N
MIPI DSI Data Negative 0	PA17	AP_MIPIDSI_DN0	1.8V	IO	N
MIPI DSI Data Negative 1	PA18	AP_MIPIDSI_DN1	1.8V	IO	N
MIPI DSI Data Negative 2	PA19	AP_MIPIDSI_DN2	1.8V	IO	N
MIPI DSI Data Negative 3	PA20	AP_MIPIDSI_DN3	1.8V	IO	N
MIPI DSI Data Positive Clock	PB16	AP_MIPIDSI_DPCLK	1.8V	IO	N
MIPI DSI Data Positive 0	PB17	AP_MIPIDSI_DP0	1.8V	IO	N
MIPI DSI Data Positive 1	PB18	AP_MIPIDSI_DP1	1.8V	IO	N
MIPI DSI Data Positive 2	PB19	AP_MIPIDSI_DP2	1.8V	IO	N
MIPI DSI Data Positive 3	PB20	AP_MIPIDSI_DP3	1.8V	IO	N

5.11 HDMI

Table 17. HDMI

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
HDMI Consumer Electronics Control *	PA29	AP_HDMI_CEC	3.3V	IO	PU
HDMI Hot Plug Detect	PB29	AP_HDMI_HPD	3.3V	I	N
HDMI Transmit Channel 0 Negative	PA32	AP_HDMI_TX0N	1.8V	O	N
HDMI Transmit Channel 0 Positive	PB32	AP_HDMI_TX0P	1.8V	O	N
HDMI Transmit Channel 1 Negative	PA31	AP_HDMI_TX1N	1.8V	O	N
HDMI Transmit Channel 1 Positive	PB31	AP_HDMI_TX1P	1.8V	O	N
HDMI Transmit Channel 2 Negative	PA30	AP_HDMI_TX2N	1.8V	O	N
HDMI Transmit Channel 2 Positive	PB30	AP_HDMI_TX2P	1.8V	O	N
HDMI Transmit Negative Clock	PA33	AP_HDMI_TXCN	1.8V	O	N
HDMI Transmit Positive Clock	PB33	AP_HDMI_TXCP	1.8V	O	N
HDMI I^2C SCL †	PAK11	AP_GPA23_HDMI_I2C_SCL	3.3V	IO	N
HDMI I^2C SDA †	PAL11	AP_GPA24_HDMI_I2C_SDA	3.3V	IO	N

*. Alternate GPIO function that can be selected by software but is not selected by hardware at power-on. See ***Table 29*** for details.

†. Not selected by default by hardware at power-on. The signal can be reassigned by software. See ***Table 30*** for details.

5.12 LVDS

Table 18. LVDS

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
LVDS Transmit Channel 0 Negative	PA22	AP_LVDS_TN0	1.8V	O	N
LVDS Transmit Channel 0 Positive	PB22	AP_LVDS_TP0	1.8V	O	N
LVDS Transmit Channel 1 Negative	PA23	AP_LVDS_TN1	1.8V	O	N
LVDS Transmit Channel 1 Positive	PB23	AP_LVDS_TP1	1.8V	O	N
LVDS Transmit Channel 2 Negative	PA24	AP_LVDS_TN2	1.8V	O	N
LVDS Transmit Channel 2 Positive	PB24	AP_LVDS_TP2	1.8V	O	N
LVDS Transmit Channel 3 Negative	PA26	AP_LVDS_TN3	1.8V	O	N
LVDS Transmit Channel 3 Positive	PB26	AP_LVDS_TP3	1.8V	O	N
LVDS Transmit Channel 4 Negative	PA27	AP_LVDS_TN4	1.8V	O	N
LVDS Transmit Channel 4 Positive	PB27	AP_LVDS_TP4	1.8V	O	N
LVDS Transmit Negative Clock	PA25	AP_LVDS_TNCLK	1.8V	O	N
LVDS Transmit Positive Clock	PB25	AP_LVDS_TPCLK	1.8V	O	N

5.13 ADC

Table 19. ADC

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
ADC Channel 0	PY1	AP_ADC0	1.8V	I	N
ADC Channel 1	PY2	AP_ADC1	1.8V	I	N
ADC Channel 2	PAA1	AP_ADC2	1.8V	I	N
ADC Channel 3	PAA2	AP_ADC3	1.8V	I	N
ADC Channel 4	PW1	AP_ADC4	1.8V	I	N
ADC Channel 5	PW2	AP_ADC5	1.8V	I	N

5.14 GPIO

Table 20. GPIO

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD *
GPIO A0	PAH2	AP_GPA0	3.3V	IO	N
GPIO A3	PAL42	AP_GPA3	3.3V	IO	N
GPIO A4	PB39	AP_GPA4	3.3V	IO	N
GPIO A5	PB40	AP_GPA5	3.3V	IO	N
GPIO A6	PAK42	AP_GPA6	3.3V	IO	N
GPIO A9	PA40	AP_GPA9	3.3V	IO	N
GPIO A10	PAK41	AP_GPA10	3.3V	IO	N
GPIO A11	PB42	AP_GPA11	3.3V	IO	N
GPIO A12	PA42	AP_GPA12	3.3V	IO	N

Table 20. GPIO (Continued)

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD *
GPIO A13	PA37	AP_GPA13	3.3V	IO	N
GPIO A14	PA39	AP_GPA14	3.3V	IO	N
GPIO A15	PA41	AP_GPA15	3.3V	IO	N
GPIO A16	PB41	AP_GPA16	3.3V	IO	N
GPIO A17	PAL41	AP_GPA17	3.3V	IO	N
GPIO A18	PAK39	AP_GPA18	3.3V	IO	N
GPIO A19	PAL40	AP_GPA19	3.3V	IO	N
GPIO A20	PAK38	AP_GPA20	3.3V	IO	N
GPIO A21	PAK40	AP_GPA21	3.3V	IO	N
GPIO A22	PAL39	AP_GPA22	3.3V	IO	N
GPIO A25	PAG2	AP_GPA25	3.3V	IO	N
GPIO A26	PAH1	AP_GPA26	3.3V	IO	N
GPIO A27	PAJ2	AP_GPA27	3.3V	IO	N
GPIO A28	PAK26	AP_GPA28	3.3V	IO	N
GPIO B8	PAK36	AP_GPB8	3.3V	IO	N
GPIO B11	PAG41	AP_GPB11	3.3V	IO	N
GPIO B14	PAK37	AP_GPB14	3.3V	IO	N
GPIO B16	PAL37	AP_GPB16	3.3V	IO	N
GPIO B18	PAG42	AP_GPB18	3.3V	IO	N
GPIO B22	PAL36	AP_GPB22	3.3V	IO	N
GPIO B23	PAL38	AP_GPB23	3.3V	IO	N
GPIO B30	PP41	AP_GPB30	3.3V	IO	–
GPIO C0	PAK34	AP_GPC0	3.3V	IO	N
GPIO C17	PAK33	AP_GPC17	3.3V	IO	N
GPIO C25	PAH41	AP_GPC25	3.3V	IO	PU
GPIO C26	PAK35	AP_GPC26	3.3V	IO	PU
GPIO C27	PAL35	AP_GPC27	3.3V	IO	PU
GPIO D8	PAL33	AP_GPD8	3.3V	IO	N
GPIO D28	PAK19	AP_GPD28	3.3V	IO	N
GPIO D31	PAL25	AP_GPD31	3.3V	IO	N
GPIO E0	PAL21	AP_GPE0	3.3V	IO	N
GPIO E1	PAK21	AP_GPE1	3.3V	IO	N
GPIO E2	PAK20	AP_GPE2	3.3V	IO	N
GPIO E3	PAL20	AP_GPE3	3.3V	IO	N
GPIO E30	PAL34	AP_GPE30	3.3V	IO	PU
GPIO E31	PAH42	AP_GPE31	3.3V	IO	PU

*. The GPIO lines can be pulled up or down by 100kΩ internal registers under register control. By default, the pull-ups and pull-downs are disabled. For details about reconfiguring the GPIO lines, refer to the *ARTIK 530/710 System Design Guide*.

The above signals can be reassigned by software to alternate functions; see *Table 29*–*Table 32* for details.

5.15 I²S

Table 21. I²S

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
I²S 0 Bit Clock *	PAK2	AP_I2S0_BCLK	3.3V	IO	N
I²S 0 Data In *	PAL1	AP_I2S0_DIN	3.3V	IO	N
I²S 0 Data Out *	PAK1	AP_I2S0_DOUT	3.3V	IO	N
I²S 0 Left/Right Clock *	PAJ1	AP_I2S0_LRCLK	3.3V	IO	N
I²S 0 Master Clock *	PAL2	AP_I2S0_MCLK	3.3V	IO	N
I²S 1 Bit Clock †	PAK27	AP_GPA30_VID1_0_I2SBCLK1	3.3V	IO	PU
I²S 1 Data In †	PAL26	AP_GPB9_I2SDIN1	3.3V	IO	N
I²S 1 Data Out †	PAL27	AP_GPB6_VID1_4_I2SDOUT1	3.3V	IO	PD
I²S 1 Left/Right Clock †	PAK25	AP_GPB0_VID1_1_I2SLRCK1	3.3V	IO	PU
I²S 1 Master Clock †	PAK26	AP_GPA28_I2SMCLK1	3.3V	IO	N

*. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See *Table 30* and *Table 31* for details.

†. Alternate GPIO function that can be selected by software but is not selected by hardware at power-on. See *Table 30* for details.

5.16 PWM

Table 22. PWM

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
PWM 0	PAL7	AP_GPD1_PWM0	3.3V	IO	N
PWM 2	PAK7	AP_GPC14_PWM2	3.3V	IO	N

The above signals can be reassigned by software to alternate functions; see *Table 30* for details.

5.17 SPI

Table 23. SPI

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
SPI 0 Clock *	PAK6	AP_SPI0_CLK	3.3V	IO	N
SPI 0 Frame *	PAL6	AP_SPI0_CS	3.3V	IO	N
SPI 0 Receive Data *	PAK5	AP_SPI0_MISO	3.3V	IO	N
SPI 0 Transmit Data *	PAL5	AP_SPI0_MOSI	3.3V	IO	N
SPI 2 Clock †	PAK4	AP_GPC9_SPI2_CLK	3.3V	IO	N
SPI 2 Frame	PAL4	AP_GPC10_SPI2_CS	3.3V	IO	PU
SPI 2 Receive Data	PAK3	AP_GPC11_SPI2_MISO	3.3V	IO	N
SPI 2 Transmit Data	PAL3	AP_GPC12_SPI2_MOSI	3.3V	IO	N

*. Alternate GPIO function that can be reassigned by software but is not selected by hardware at power-on; see *Table 30* for details.

†. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See *Table 30* for details.

5.18 UART

Table 24. UART

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
UART 0 Receive Data	PAL24	AP_UART_RX0	3.3V	IO	N
UART 0 Transmit Data	PAK24	AP_UART_TX0	3.3V	IO	N
UART 3 Receive Data	PAL22	AP_UART_RX3	3.3V	IO	N
UART 3 Transmit Data	PAK22	AP_UART_TX3	3.3V	IO	N
UART 4 Receive Data	PAL23	AP_UART_RX4	3.3V	IO	N
UART 4 Transmit Data	PAK23	AP_UART_TX4	3.3V	IO	N

The above signals can be reassigned by software to alternate functions; see *Table 30* for details.

5.19 I²C

Table 25. I²C

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
I²C SCL 0 *	PAK10	AP_GPD2_SCL0	3.3V	IO	PU
I²C SDA 0 *	PAL10	AP_GPD3_SDA0	3.3V	IO	PU
I²C SCL 1 *	PAK9	AP_GPD4_SCL1	3.3V	IO	PU
I²C SDA 1 *	PAL9	AP_GPD5_SDA1	3.3V	IO	PU
I²C SCL 2 *	PAK8	AP_GPD6_SCL2	3.3V	IO	PU
I²C SDA 2 *	PAL8	AP_GPD7_SDA2	3.3V	IO	PU

*. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See *Table 30* for details.

5.20 JTAG

Table 26. JTAG

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
JTAG NTRST	PAE1	AP_NTRST	3.3V	IO	PD
JTAG TCK	PAC1	AP_TCK	3.3V	IO	PD
JTAG TDI	PAD2	AP_TDI	3.3V	IO	PU
JTAG TDO	PAD1	AP_TDO	3.3V	IO	N
JTAG TMS	PAC2	AP_TMS	3.3V	IO	PU

The above signals can be reassigned by software to alternate functions; see *Table 31* for details.

5.21 Booting

Table 27. Booting

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
Booting Configuration 1	PAK32	AP_GPB13_SD0_BOOT	3.3V	I	PU
Booting Configuration 2	PAL32	AP_GPB15_SD1_BOOT	3.3V	I	PD
Booting Configuration 3	PAL31	AP_GPB4_VID1_3_BOOT	3.3V	I	PU

NOTE If a preferred boot device fails, the above pins select whether secondary and/or tertiary boot options are available. For details, see *Booting Selection*.

The above signals can be reassigned by software to alternate functions; see *Table 30* for details.

5.22 Miscellaneous

Table 28. Miscellaneous

Function	Ball Loc.	Ball Name	Voltage	I/O	PU/PD
VDD Power On	PAL19	AP_VDDPWRON	3.3V	O	N

6 GPIO Alternate Functions

A number of the GPIOs can be programmed to have alternate functions beyond their default behavior using the GPIO API provided in the SW development environment. *Table 29–Table 32* provide the alternate functions of all the GPIOs that are available on the PADs of the ARTIK 530/530s Module that can be user programmed.

NOTE In the following tables, the hardware power-up default functions are shown emboldened. Software may subsequently select an alternate function. Cells that are grayed out have either no function associated with them or the function is not supported on the ARTIK 530/530s Module.

Table 29. GPIO Alternate Functions—North Side

Ball Loc.	Ball Name	Function 0	Function 1	Function 2	Function 3	Group
PA1	GMAC_TXEN	GPIOE11	**GMAC_TXEN**	–	–	GMAC
PA2	GMAC_TXD1	GPIOE8	**GMAC_TXD1**	–	–	GMAC
PA3	GMAC_TXD3	GPIOE10	**GMAC_TXD3**	–	–	GMAC
PA5	GMAC_GTXCLK	GPIOE24	**GMAC_GTXCLK**	–	–	GMAC
PA6	GMAC_RXDV	GPIOE19	**GMAC_RXDV**	SPITXD1	–	GMAC
PA7	GMAC_RXD2	GPIOE16	**GMAC_RXD2**	–	–	GMAC
PA8	GMAC_RXD0	GPIOE14	**GMAC_RXD0**	SPICLK1	–	GMAC
PA29	AP_HDMI_CEC	**SA3**	GPIOC3	HDMI_CEC	SDnRST0	HDMI
PA37	AP_GPA13	**GPIOA13**	DISD12	–	–	GPIO
PA39	AP_GPA14	**GPIOA14**	DISD13	–	–	GPIO
PA40	AP_GPA9	**GPIOA9**	DISD8	–	–	GPIO
PA41	AP_GPA15	**GPIOA15**	DISD14	–	–	GPIO
PA42	AP_GPA12	**GPIOA12**	DISD11	–	–	GPIO
PB2	GMAC_TXD0	GPIOE7	**GMAC_TXD0**	VIVSYNC1	–	GMAC
PB3	GMAC_TXD2	GPIOE9	**GMAC_TXD2**	–	–	GMAC
PB4	GMAC_MDC	GPIOE20	**GMAC_MDC**	–	–	GMAC
PB5	GMAC_RXCLK	GPIOE18	**GMAC_RXCLK**	SPIRXD1	–	GMAC
PB6	GMAC_RXD3	GPIOE17	**GMAC_RXD3**	–	–	GMAC
PB7	GMAC_RXD1	GPIOE15	**GMAC_RXD1**	SPIFRM1	–	GMAC
PB8	GMAC_MDIO	GPIOE21	**GMAC_MDIO**	–	–	GMAC
PB39	AP_GPA4	**GPIOA4**	DISD3	–	–	GPIO
PB40	AP_GPA5	**GPIOA5**	DISD4	–	–	GPIO
PB41	AP_GPA16	**GPIOA16**	DISD15	–	–	GPIO
PB42	AP_GPA11	**GPIOA11**	DISD10	–	–	GPIO

Table 30. GPIO Alternate Functions—South Side

Ball Loc.	Ball Name	Function 0	Function 1	Function 2	Function 3	Group
PAK1	AP_I2S0_DOUT	GPIOD9	**I2SDOUT0**	AC97_DOUT	–	I2S0
PAK2	AP_I2S0_BCLK	GPIOD10	**I2SBCLK0**	AC97_BCLK	–	I2S0
PAK3	AP_GPC11_SPI2_MISO	SA11	GPIOC11	**SPIRXD2**	USB2.0OTG_DrvVBUS	SPI2
PAK4	AP_GPC9_SPI2_CLK	SA9	GPIOC9	**SPICLK2**	–	SPI2
PAK5	AP_SPI0_MISO	**GPIOD0**	SPIRXD0	PWM3	–	SPI0
PAK6	AP_SPI0_CLK	**GPIOC29**	SPICLK0	–	–	SPI0
PAK7	AP_GPC14_PWM2	SA14	GPIOC14	**PWM2**	VICLK2	PWM
PAK8	AP_GPD6_SCL2	GPIOD6	**SCL2**	–	–	I^2C
PAK9	AP_GPD4_SCL1	GPIOD4	**SCL1**	–	–	I^2C
PAK10	AP_GPD2_SCL0	GPIOD2	**SCL0**	ISO7816	–	I^2C
PAK11	AP_GPA23	**GPIOA23**	DISD22	–	–	I^2C
PAK19	AP_GPD28	**GPIOD28**	VID0_0	TSIDATA1_0	SA24	GPIO
PAK20	AP_GPE2	**GPIOE2**	VID0_6	TSIDATA1_6	–	GPIO
PAK21	AP_GPE1	**GPIOE1**	VID0_5	TSIDATA1_5	–	GPIO
PAK22	AP_UART_TX3	GPIOD21	**UARTTXD3**	SDnCD1	–	UART
PAK23	AP_UART_TX4	SD13	GPIOB29	TSIDATA0_5	**UARTTXD4**	UART
PAK24	AP_UART_TX0	**GPIOD18**	UARTTXD0	ISO7816	SDWP2	UART
PAK25	AP_GPB0_VID1_1_I2SLRCK1	**GPIOB0**	VID1_1	SDEX1	I2SLRCLK1	I2S1
PAK26	AP_GPA28_I2SMCLK1	**GPIOA28**	VICLK1	I2SMCLK2	I2SMCLK1	I2S1
PAK27	AP_GPA30_VID1_0_I2SBCLK1	**GPIOA30**	VID1_0	SDEX0	I2SBCLK1	I2S1
PAK28	AP_SD0_CMD	GPIOA31	**SDCMD0**	–	–	SD/MMC
PAK29	AP_SD0_D1	GPIOB3	**SDDAT0_1**	–	–	SD/MMC
PAK30	AP_SD0_CLK	GPIOA29	**SDCLK0**	–	–	SD/MMC
PAK32	AP_GPB13_SD0_BOOT	**SD0**	GPIOB13	–	–	BOOTING
PAK33	AP_GPC17	SA17	**GPIOC17**	TSIDP0	VID2_0	GPIO
PAK34	AP_GPC0	SA0	**GPIOC0**	TSERR0	–	GPIO
PAK35	AP_GPC26	RDNWR	**GPIOC26**	–	–	GPIO
PAK36	AP_GPB8	**GPIOB8**	VID1_5	SDEX5	I2SDOUT2	GPIO
PAK37	AP_GPB14	RnB0	RnB1	**GPIOB14**	–	GPIO
PAK38	AP_GPA20	**GPIOA20**	DISD19	–	–	GPIO
PAK39	AP_GPA18	**GPIOA18**	DISD17	–	–	GPIO
PAK40	AP_GPA21	**GPIOA21**	DISD20	–	–	GPIO
PAK41	AP_GPA10	**GPIOA10**	DISD9	–	–	GPIO
PAK42	AP_GPA6	**GPIOA6**	DISD5	–	–	GPIO
PAL1	AP_I2S0_DIN	GPIOD11	**I2SDIN0**	AC97_DIN	–	I2S0
PAL2	AP_I2S0_MCLK	GPIOD13	**I2SMCLK0**	AC97_nRST	–	I2S0
PAL3	AP_GPC12_SPI2_MOSI	SA12	GPIOC12	**SPITXD2**	SDnRST2	SPI2
PAL4	AP_GPC10_SPI2_CS	SA10	GPIOC10	**SPIFRM2**	–	SPI2
PAL5	AP_SPI0_MOSI	**GPIOC31**	SPITXD0	–	–	SPI0
PAL6	AP_SPI0_CS	**GPIOC30**	SPIFRM0	–	–	SPI0
PAL7	AP_GPD1_PWM0	GPIOD1	**PWM0**	SA25	–	PWM
PAL8	AP_GPD7_SDA2	GPIOD7	**SDA2**	–	–	I^2C

Table 30. GPIO Alternate Functions—South Side (Continued)

Ball Loc.	Ball Name	Function 0	Function 1	Function 2	Function 3	Group
PAL9	AP_GPD5_SDA1	GPIOD5	**SDA1**	–	–	I^2C
PAL10	AP_GPD3_SDA0	GPIOD3	**SDA0**	ISO7816	–	I^2C
PAL11	AP_GPA24_HDMI_I2C_SDA	**GPIOA24**	DISD23	–	–	I^2C
PAL20	AP_GPE3	**GPIOE3**	VID0_7	TSIDATA1_7	–	GPIO
PAL21	AP_GPE0	**GPIOE0**	VID0_4	TSIDATA1_4	–	GPIO
PAL22	AP_UART_RX3	GPIOD17	**UARTRXD3**	–	–	UART
PAL23	AP_UART_RX4	SD12	GPIOB28	TSIDATA0_4	**UARTRXD4**	UART
PAL24	AP_UART_RX0	**GPIOD14**	UARTRXD0	ISO7816	–	UART
PAL25	AP_GPD31	**GPIOD31**	VID0_3	TSIDATA1_3	–	GPIO
PAL26	AP_GPB9_I2SDIN1	**GPIOB9**	VID1_6	SDEX6	I2SDIN1	I2S1
PAL27	AP_GPB6_VID1_4_I2SDOUT1	**GPIOB6**	VID1_4	SDEX4	I2SDOUT1	I2S1
PAL28	AP_SD0_D3	GPIOB7	**SDDAT0_3**	–	–	SD/MMC
PAL29	AP_SD0_D2	GPIOB5	**SDDAT0_2**	–	–	SD/MMC
PAL30	AP_SD0_D0	GPIOB1	**SDDAT0_0**	–	–	SD/MMC
PAL31	AP_GPB4_VID1_3_BOOT	GPIOB4	**VID1_3**	SDEX3	I2SLRCLK2	BOOTING
PAL32	AP_GPB15_SD1_BOOT	**SD1**	GPIOB15	–	–	BOOTING
PAL33	AP_GPD8	**GPIOD8**	PPM	–	–	GPIO
PAL34	AP_GPE30	NSOE	**GPIOE30**	–	–	GPIO
PAL35	AP_GPC27	NSDQM	**GPIOC27**	–	–	GPIO
PAL36	AP_GPB22	SD6	**GPIOB22**	–	–	GPIO
PAL37	AP_GPB16	NNFOE0	NNFOE1	**GPIOB16**	–	GPIO
PAL38	AP_GPB23	SD7	**GPIOB23**	–	–	GPIO
PAL39	AP_GPA22	**GPIOA22**	DISD21	–	–	GPIO
PAL40	AP_GPA19	**GPIOA19**	DISD18	–	–	GPIO
PAL41	AP_GPA17	**GPIOA17**	DISD16	–	–	GPIO
PAL42	AP_GPA3	**GPIOA3**	DISD2	–	–	GPIO

Table 31. GPIO Alternate Functions—East Side

Ball Loc.	Ball Name	Function 0	Function 1	Function 2	Function 3	Group
PAC1	AP_TCK	**TCLK**	GPIOE28	–	–	JTAG
PAC2	AP_TMS	**TMS**	GPIOE26	–	–	JTAG
PAD1	AP_TDO	**TDO**	GPIOE29	–	–	JTAG
PAD2	AP_TDI	**TDI**	GPIOE27	–	–	JTAG
PAE1	AP_NTRST	**NTRST**	GPIOE25	–	–	JTAG
PAG2	AP_GPA25	**GPIOA25**	DISVSYNC	–	–	GPIO
PAH1	AP_GPA26	**GPIOA26**	DISHSYNC	–	–	GPIO
PAH2	AP_GPA0	**GPIOA0**	DISCLK	–	–	
PAJ1	AP_I2S0_LRCLK	GPIOD12	**I2SLRCLK0**	AC97_SYNC	–	I2S0
PAJ2	AP_GPA27	**GPIOA27**	DISDE	–	–	

Table 32. GPIO Alternate Functions—West Part

Ball Loc.	Ball Name	Function 0	Function 1	Function 2	Function 3	Group
PP41	AP_GPIOB30	SD14	**GPIOB30**	TSIDATA0_6	–	GPIO
PAG41	AP_GPB11	**CLE0**	CLE1	GPIOB11	–	GPIO
PAG42	AP_GPB18	NNFWE0	nNFWE1	**GPIOB18**	–	GPIO
PAH41	AP_GPC25	NSWAIT	**GPIOC25**	SPDIFTX	–	GPIO
PAH42	AP_GPE31	NSWE	**GPIOE31**	–	–	GPIO

7 Booting Selection

The ARTIK 530/530s Module supports a variety of booting scenarios as depicted in *Table 33*. The table describes the values of the boot-configuration pad signals needed to initiate the booting scenarios. When nothing is done, the default booting scenario is Configuration Option 1. In this case, the primary booting device is eMMC. If the primary booting device fails, the secondary booting device (SD0) will attempt to boot the module. If the secondary booting device fails, the tertiary booting device will boot the module.

Table 33. Boot Selection Configuration

Config. Option	Boot Configuration Signals *			Primary Booting Device	Secondary Booting Device	Tertiary Booting Device
	AP_GPB13_ SD0_BOOT	AP_GPB15_ SD1_BOOT	AP_GPB4_ VID1_3_ BOOT			
1	High	Low	High	eMMC	SD0	USB OTG Device
2	High	Low	Low	SD0	USB OTG Device	–
3	Low	High	X	USB OTG Device	–	–

*. Internal pull-up and pull-down resistors automatically select Config Option 1 by default. External pull-up and pull-down resistors are required to select configuration options 2 and 3. The recommended resistor value is 10kΩ.

8 Power Sequence

Figure 4 below shows the ARTIK 530/530s Module Power-On Sequence (Timing).

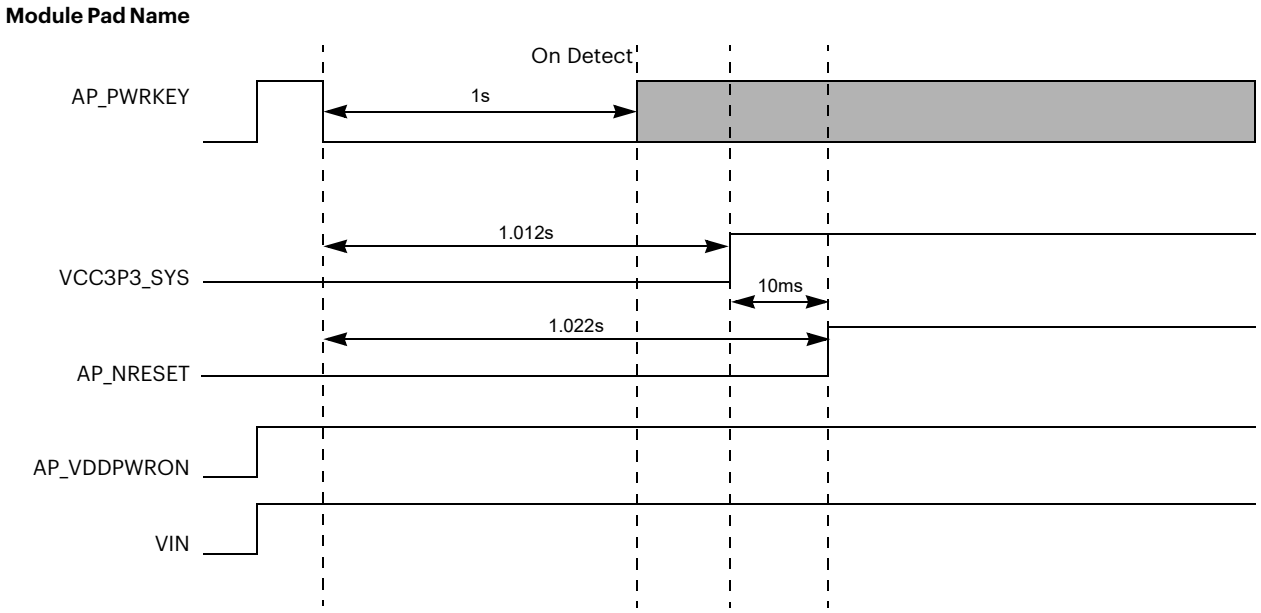

Figure 4. ARTIK 530/530s Module Power-On Sequence (Timing) Diagram

9 Power States

Figure 5 shows the Power Management state diagram. In this diagram, the entry and WAKEUP conditions for each power down mode are given.

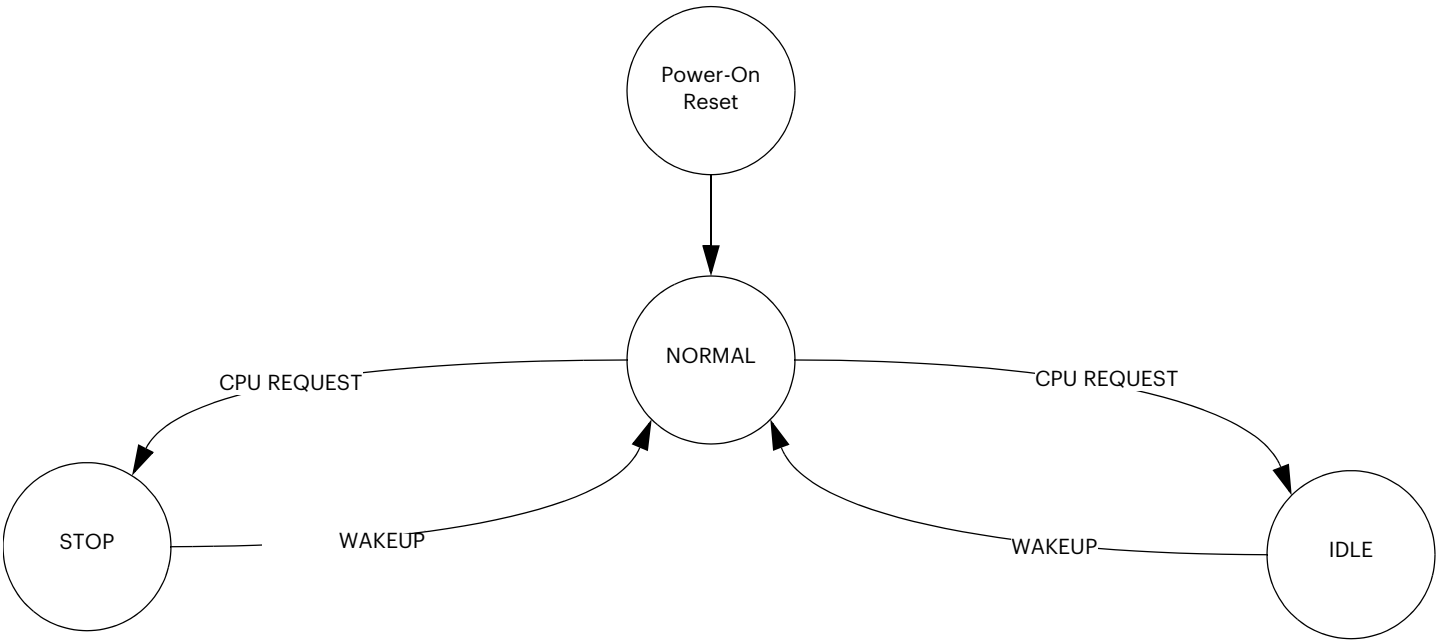

Figure 5. ARTIK 530/530s Module Power Management State Diagram

The following Modes of operation can be distinguished:

- NORMAL Mode
  - Everything is running, this is the normal mode of operation when applications are executed on the ARM cores
- IDLE Mode
  - CPU clocks are turned off
  - IDLE state can be initiated by CPU using Software API
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - GPIO Interrupt, RTC Interrupt, AliveGPIO Interrupt (see PAE2, PAF:[1,2]), External IRQ
- STOP Mode
  - PLLs are turned off, DRAM goes into self-refresh
  - STOP state can be initiated by CPU using Software API
  - Certain WAKEUP sources can be used to transition to NORMAL Mode
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - RTC Interrupt, AliveGPIO Interrupt

For more information on how to access discussed WAKEUP mechanisms like AliveGPIO interrupts, GPIO Interrupts, RTC Interrupts and External Interrupts, refer to the Software User Guide.

10 Antenna Connections

Two antennas are required to use the full set of radio communication links on the ARTIK 530/530s Module. One supports the combination of Wi-Fi/Bluetooth, and the other is dedicated to Zigbee.

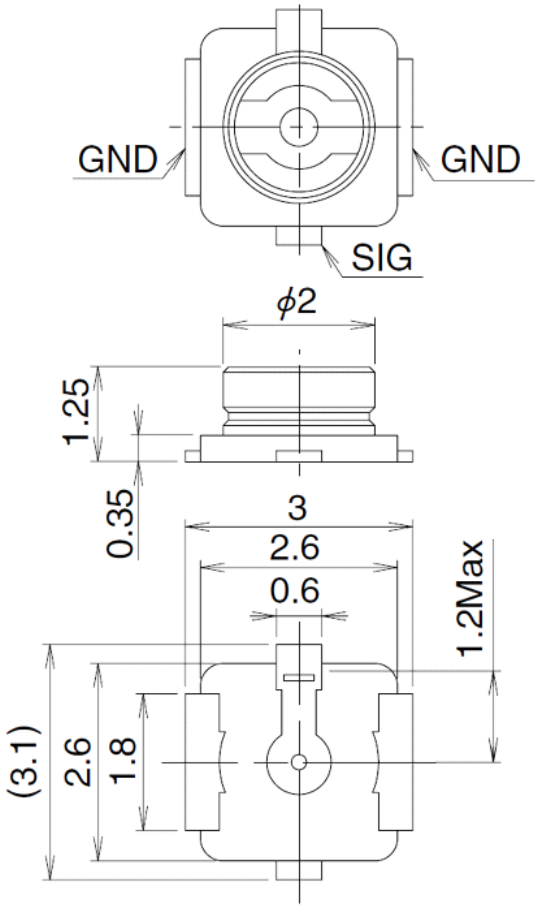

Figure 6. RF Connector for Bluetooth/Wi-Fi and Zigbee

The U.FL-R-SMT Hirose connector is used for both the Bluetooth/Wi-Fi and the Zigbee antenna connectors on the ARTIK 530/530s Module.

The mechanical size of the connector (receptacle) is described in *Figure 6*. For suggestions on mating the plug and more details on the connector, contact Hirose Electric Co., LTD.

11 Electrical Specifications

11.1 Absolute Maximum Ratings

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 34. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Units
Main power supply	VIN	–	–0.3	6.0	V
DC input/output voltage	PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	3.3V Buffer	–0.5	3.8	
	PAK:[12,13,14] PAL:[12,13]	5V Tolerant buffer	–0.3	5.3	
	PAK:[15] PAL:[15]	Non 5V Tolerant Buffer	–0.3	3.6	
	PAL:[19] PAF:[1] PAG:[1]	–	–0.3	3.8	
	PAL:[14]	Voltage at Pin	–0.5	3.8	V
DC Input/output current	PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	–	–20	20	mA
	PAK:[12,13,14,15] PAL:[12,13]	–	–50	50	mA
	PAL:[14]	Current at Pin	–1	1	mA

11.2 Power Supply Operating Voltage Range

Table 35. Power Supply Operating Voltage Range

Parameter	Symbol	Min	Typ	Max	Units
Main Power Supply	VIN PV:[41,42],PW:[41,42],PY:[41,42],PAA:[41,42],PAB:[41,42]	3.7	4.2	5.0	V

11.3 Power/Current Consumption

The values in this table are nominal. Measurements were taken on sample boards at room temperature using a 4.2V system power supply.

Table 36. ARTIK 530/530s Module Power/Current Consumption

No.	Category	Scenario		I (mA)	Peak/Typ	Condition
1	Boot	AP boot		700	Peak	Peek current during boot-up
				450	Typ	Average current during boot-up
2	Idle	Idle		140	Typ	Idle current
3	Sleep	Sleep		20	Typ	Sleep current
4	Storage	Large file transfer	eMMC to SD Card	230	Typ	Copying 512MB test file from eMMC to SD
5			SD Card to eMMC	270	Typ	Copying 512MB test file from SD to eMMC
6	Connectivity	Bluetooth	Transmit	170	Typ	Transfer test file using `obexftp` from the device
7			Receive	160	Typ	Receive test file using `obexftp` from the Android phone
8		Wi-Fi	Transmit	430	Typ	Transfer packet using `iperf3` (802.11n)
9			Receive	320	Typ	Receive packet using `iperf3` (802.11n)
10		802.15.4 for Zigbee	Transmit	150	Typ	Transfer packet using `ember` tool
11			Receive	150	Typ	Receive packet using `ember` tool
12	Multimedia	Audio play		150	Typ	Playback audio file using `mplayer` (pcm, 2ch, 48000Hz)
13		Recode audio		140	Typ	Record audio using `arecord` (pcm, 2ch, 48000Hz)
14		Display picture		180	Typ	Display picture (R/G/B, 720*1280)
15		Display video		330	Typ	Playback movie clip (big_buck_bunny_720p_50mb)
16		Record video		300	Typ	Record video using `ffmpeg` (1280*720, 3072k)
17		Live streaming from Camera		310	Typ	Camera preview using `ffmpeg` (1280x960)
18		Live streaming over Wi-Fi		320	Typ	Streaming video using `ffserver`/`ffmpeg` (640*480)
19	CPU Load	Running one core at 100% load		240	Typ	Running while() loop
		Running two cores at 100% load		320		
		Running three cores at 100% load		400		
		Running all cores at 100% load		480		

11.4 DC Electrical Characteristics

The DC characteristics for the GPIO pins of the ARTIK 530/530s Module are listed in *Table 37*. Use the parameters from *Table 37* to determine maximum DC loading and to determine maximum transition times for a given load.

Table 37. I/O DC Electrical Characteristics GPIO

GPIO Ball Coordinates	Parameter		Condition *		Min	Typ	Max	Units
PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42] PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PP:[41] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,41,42] PAH:[1,2,41,42] PAJ:[1,2]	V_{TOL}	Tolerant external voltage	V_{DD} Power Off & On		–	–	3.60	V
	V_{IH}	High Level Input Voltage CMOS Interface	–		2.31	–	3.60	V
	V_{IL}	Low Level Input Voltage CMOS Interface	V_{DD} = 3.3V ± 10%		–0.3	–	0.70	V
	ΔV	Hysteresis Voltage	–		0.15	–		V
	I_{IH}	High Level Input Current						
		Input Buffer	$V_{IN} = V_{DD}$	V_{DD} Power On	–3	–	3	µA
				V_{DD} Power Off & SNS = 0	–5	–	5	
		Input Buffer with pull-down	$V_{IN} = V_{DD}$	V_{DD} = 3.3V ± 10%	15	40	80	
	I_{IL}	Low Level Input Current						
		Input Buffer	$V_{IN} = V_{SS}$	V_{DD} Power On & Off	–3	–	3	µA
		Input Buffer with pull-up	$V_{IN} = V_{SS}$	V_{DD} = 3.3V ± 10%	–15	–40	–110	
	V_{OH}	Output High Voltage	I_{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA		2.64	–	3.30	V
	V_{OL}	Output Low Voltage	I_{OH} = -1.8mA, -3.6mA, -7.2mA, -10.8mA		0	–	0.66	
	I_{OZ}	Output Hi-Z current	–		–5	–	5	µA
	C_{IN}	Input capacitance	Any input and bi-directional buffers		–	–	5	pF
	C_{OUT}	Output capacitance	Any output buffer		–	–	5	pF

*. Operating conditions: V_{DD} = 3.3V, V_{ext} = 3.0 to 3.6 V, T_j = –40 to 125 °C (Junction Temperature), 3.3V-tolerant

Table 38. I/O DC Electrical Characteristics 802.15.4

Ball Coordinates	Symbol	Parameter	Condition	Min	Typ	Max	Units
PAK:[12,13,14,15] PAL:[12,13,15]	**Input Voltage Levels**						
	V_{IL}	V_{IL} input logic level low V_{DD}=3.3V		–	–	0.70	V
	V_{IH}	V_{IH} input logic level high V_{DD}=3.3V		2.31	–	–	V
	Output Voltage Levels						
	$V_{OL[3mA]}$	V_{OL} output logic level low V_{DD}=3.3V, I_{OL}=3ma, weak driver		–	–	0.66	V
	$V_{OH[-3mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OH}=–3ma, weak driver		2.64	–	–	V
	$V_{OH[20mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OL}=20ma, strong driver		–	–	0.66	V
	$V_{OH[-20mA]}$	V_{OH} output logic level high V_{DD}=3.3V, I_{OL}=–20ma, strong driver		2.64	–	–	V

Table 38. I/O DC Electrical Characteristics 802.15.4 (Continued)

Ball Coordinates	Symbol	Parameter	Condition	Min	Typ	Max	Units
PAL:[14]	I_Q	Quiescent Current	Static Inputs and Outputs	–	1.00	–	µA
	V_O	Maximal voltage applied to PIN in High-Impedance State	–	–	–	3.30	V
	V_{IH}	High Level Input Voltage	Logic input at V_{DD}=3.3V	1.84	–	3.30	
	V_{IL}	Low Level Input Voltage	Logic input at V_{DD}=3.3V	–	–	1.255	
	I_{IH}	High Level Input Current	Logic input V_{IN}=V_{DD}=3.3V	–1.00	–	1.00	µA
	I_{IL}	Low Level Input Current	Logic input V_{IN}=0V	–1.00	–	1.00	
	V_{OH}	High Level Output Voltage	Push-Pull & PMOS OD, I_{OL}=3mA, 1× Driver at V_{DD}=3.3V	2.721	3.108	–	V
	V_{OL}	Low Level Output Voltage	Push-Pull, IOL=3mA, 1× Driver at VDD=3.3V		0.175	0.257	
	I_{OH}	High Level Output Current	Push-Pull & PMOS OD, V_{OH}=2.4V, 1× Driver at V_{DD}=3.3V	5.774	11.066	–	mA
	I_{OL}	Low Level Output Current	Push-Pull, V_{OL}=0.4V, 1× Driver at V_{DD}=3.3V	4.491	6.438	–	

Table 39. I/O DC Electrical Characteristics PMIC

Ball Coordinates	Symbol	Parameter	Condition	Min	Typ	Max	Units
PAG:[1]	V_{OL}	Open drain, I_{OUT}=2mA	–	–	–	0.40	V
	V_{OH}	Open drain, I_{OUT}=2mA		–	–	VIN	V
PAF:[1],PAL:[19]	V_{IL}	Input only : Low level input voltage	–	–	–	0.40	V
	V_{IH}	Input only : High level input voltage		1.40	–	VIN	V

Table 40. I/O DC Electrical Characteristics PCM Signals

Ball Coordinates	Symbol	Parameter	Condition	Min	Typ	Max	Unit
PAJ:[39,40,41,42]	V_{IH}	High-level input voltage	–	2.31	–	3.70	V
	V_{IL}	Low-level input voltage	–	–0.40	–	0.99	
	V_{OH}	Output High voltage	–	2.90	–	–	V
	V_{OL}	Output Low voltage	–	–	–	0.40	

Table 41. GPIO Pull-up Resistor Current

Ball Coordinates	Pull Up	Min	Typ	Max
PA:[1,2,3,5,6,7,8,29,37,39,40,41,42] PB:[2,3,4,5,6,7,8,39,40,41,42]	Enabled (where every GPIO has a 100kΩ internal pull-up resistor).	10	33	72
PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42] PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42] PAC:[1,2] PAD:[1,2] PAE:[1] PAG:[2,42] PAH:[1,2,42] PAJ:[1,2]	Disabled (default)	–	–	0.1

Table 42. Power-on Reset Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{RESW}	Reset assert time after clock stabilization	40	–	–	ns

11.5 AC Electrical Characteristics

AC characteristics covered in this section are preliminary and are likely to change.

11.5.1 SD/MMC AC Electrical Characteristics

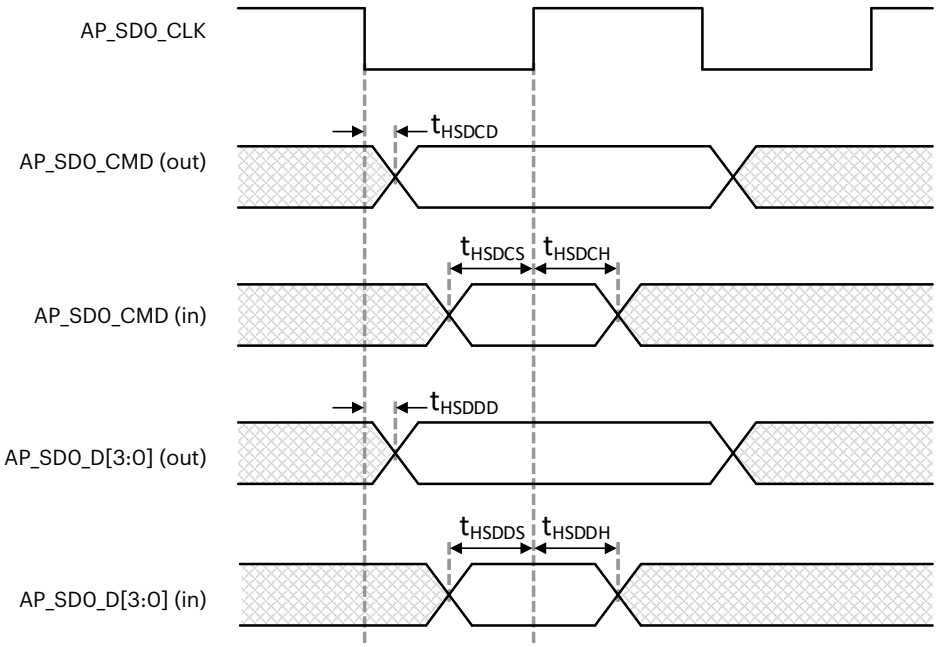

Figure 7. High-Speed SD/MMC Interface Timing

The following table assumes V_{DDINT} = 1.0V ± 5%, T_J = –25 to 85°C, V_{DDmmc} = 3.3V ± 5 %, 2.5V ± 5%, 1.8V ± 5%

Table 43. High-Speed SD/MMC Interface Transmit/Receive Timing Constants

Symbol	Parameter	Min	Typ	Max	Unit
t_{HSDCD}	SD command output delay time	–	–	4.0	ns
t_{HSDCS}	SD command input setup time	4.0	–	–	
t_{HSDCH}	SD command input hold time	0	–	–	
t_{HSDDD}	SD data output delay time	–	–	4.0	
t_{HSDDS}	SD data input setup time	4.0	–	–	
t_{HSDDH}	SD data input hold time	0	–	–	

11.5.2 SPI AC Electrical Characteristics

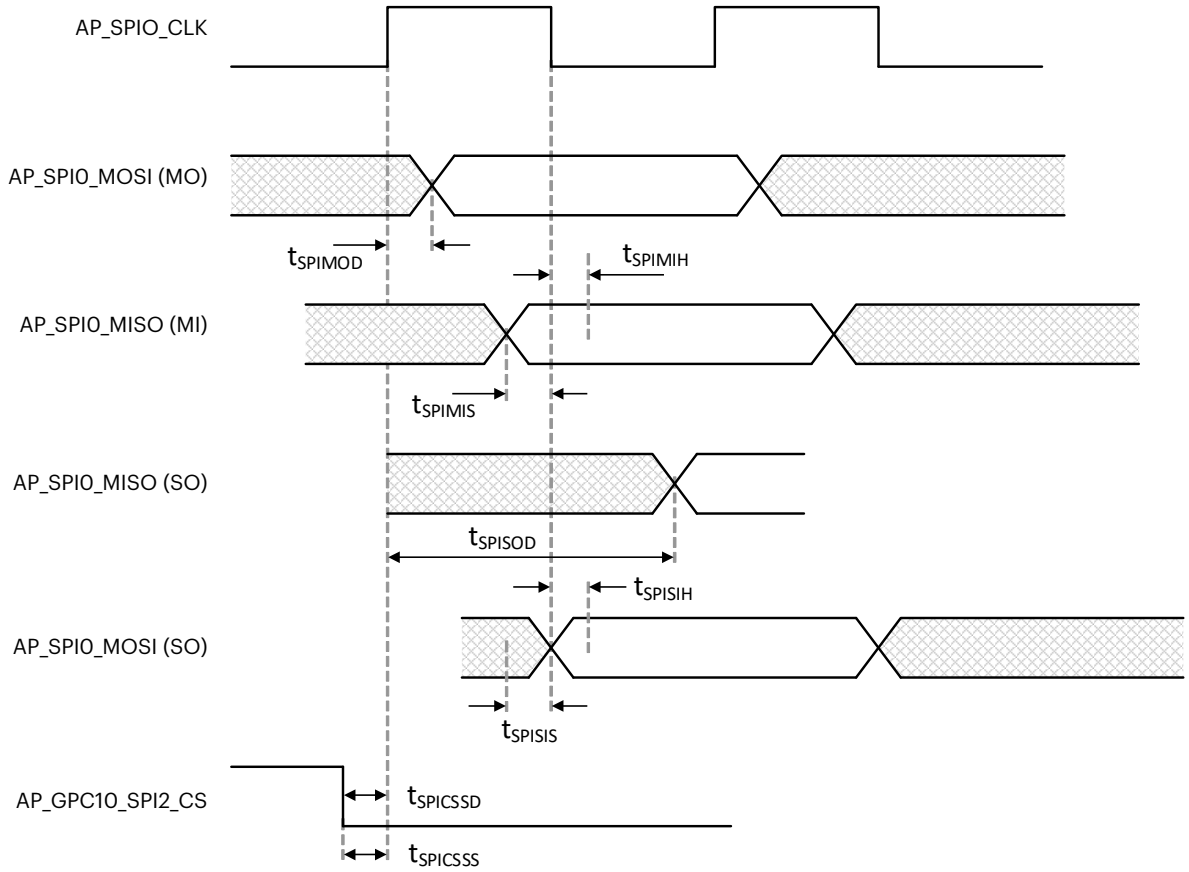

Figure 8. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A))

The following table assumes V_{DDINT} = 1.0 V ± 5%, T_J = –25 to 85 °C, V_{DDext} = 1.8 V ± 10%, load = 15pF.

Table 44. SPI Interface Transmit/ Receive Timing Constants with 15pF Load

Parameter		Symbol	Min.	Typ.	Max.	Units
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	12	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		7	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		2	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		–3	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	2	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	17	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	4	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		–2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	3	–	–	
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	7	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	5	–	–	

NOTE

$SPICLK_{out}$ = 50 MHz

- $t_{SPIMIS,CH0}$ = 12 – (cycle period/4) × FB_CLK_SEL
- $t_{SPIMIS,CH1}$ = 13 – (cycle period/4) × FB_CLK_SEL

The following table assumes V_{DDINT} = 1.0V ± 5%, T_J = –25 to 85°C, V_{DDext} = 3.3V ± 10%, load = 30pF.

Table 45. SPI Interface Transmit/Receive Timing Constants with 30pF Load

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ch 0	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	6	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	13	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		8	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		3	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		–2	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	ns
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	18	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	
Ch 1	SPI MOSI Master Output Delay time	t_{SPIMOD}	–	–	5	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 00)	t_{SPIMIS}	14	–	–	ns
	SPI MISO Master Input Setup time (FB_CLK_SEL = 01)		9	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 10)		4	–	–	
	SPI MISO Master Input Setup time (FB_CLK_SEL = 11)		–1	–	–	
	SPI MISO Master Input Hold time	t_{SPIMIH}	5	–	–	
	SPI MOSI Slave Input Setup time	t_{SPISIS}	4	–	–	
	SPI MOSI Slave Input Hold time	t_{SPISIH}	5	–	–	ns
	SPI MISO Slave Output Delay time	t_{SPISOD}	–	–	19	
	SPI nSS Master Output Delay time	$t_{SPICSSD}$	8	–	–	
	SPI nSS Slave Input Setup time	$t_{SPICSSS}$	6	–	–	

NOTE

$SPICLK_{out}$ = 50 MHz

- $t_{SPIMIS,CH0}$ = 12 – (cycle period/4) × FB_CLK_SEL
- $t_{SPIMIS,CH1}$ = 13 – (cycle period/4) × FB_CLK_SEL

11.5.3 I²C AC Electrical Characteristics

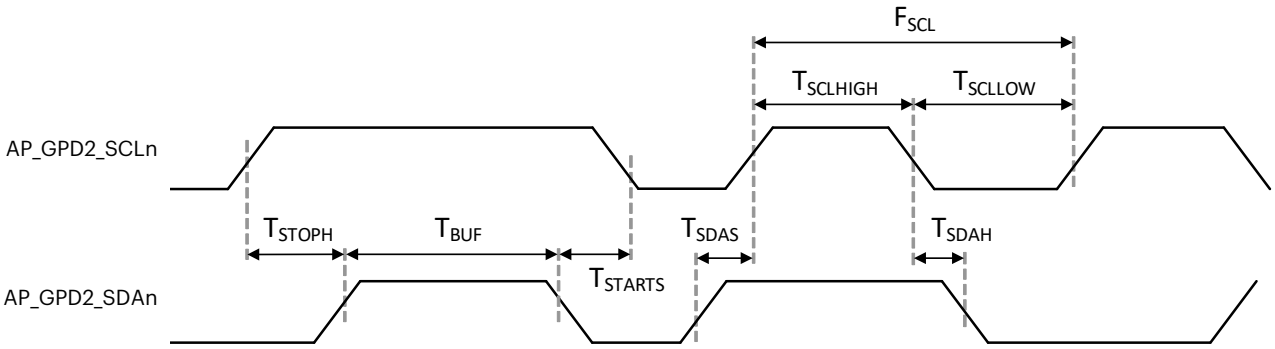

Figure 9. I²C Interface Timing

The following table assumes V_{DDINT}, V_{DDarm} = 1.1V ± 5%, T_J = –25 to 85°C, V_{DDext} = 3.3 V ± 10%

Table 46. I²C BUS Controller Module Signal Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	F_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$T_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	T_{SCLLOW}	std. 4.7 fast 1.3	–	–	
Bus free time between STOP and START	T_{BUF}	std 4.7 fast 1.3	–	–	
START hold time	T_{STARTS}	std. 4.0 fast 0.6	–	–	
SDA hold time	T_{SDAH}	std. 0 fast 0	–	std. fast 0.9	
SDA setup time	T_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	T_{STOPH}	std. 4.0 fast 0.6	–	–	µs

Modes: std. refers to Standard Mode and fast refers to Fast Mode.

NOTE

- I²C data hold time (t_{SDAH}) is minimum 0ns for standard/fast bus mode as defined in I²C specification v2.1. Check whether the data hold time of your I²C device is 0ns or not.
- The I²C controller supports I²C bus device only (standard/fast bus mode), and does not support a C-bus device.

11.6 RF Electrical Characteristics

All performance numbers related to 802.11 for Wi-Fi, Bluetooth, and 802.15.4 for Zigbee mentioned in this section are preliminary and likely to change once module characterization has taken place.

11.6.1 Wi-Fi, 2.4GHz Receiver RF Specifications

Table 47. Wi-Fi, 2.4GHz Receiver RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2400	–	2500	MHz
Minimum receiver sensitivity in 802.11b mode (2.4GHz)					
1Mbps	PER < 8%, Packet size = 1024 bytes	–	–	–	dBm
2Mbps		–	–	–	dBm
5.5Mbps		–	–	–	dBm
11Mbps		–	–	–	dBm
Minimum receiver sensitivity in 802.11g mode (2.4GHz)					
6Mbps	PER < 10%, Packet size= 1024 bytes	–	–	–	dBm
9Mbps		–	–	–	dBm
12Mbps		–	–	–	dBm
18Mbps		–	–	–	dBm
24Mbps		–	–	–	dBm
36Mbps		–	–	–	dBm
48Mbps		–	–	–	dBm
54Mbps		–	–	–	dBm
Minimum receiver sensitivity in 802.11n mode (2.4GHz)					
MCS 0	PER<10%, Packet size= 4096 bytes, GF, 800ns GI, Non-STBC	–	–	–	dBm
MCS 1		–	–	–	dBm
MCS 2		–	–	–	dBm
MCS 3		–	–	–	dBm
MCS 4		–	–	–	dBm
MCS 5		–	–	–	dBm
MCS 6		–	–	–	dBm
MCS 7		–	–	–	dBm

11.6.2 Wi-Fi, 2.4GHz Transmitter RF Specifications

Table 48. Wi-Fi, 2.4GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Linear output power					
Maximum output power in 802.11b mode	As specified in IEEE802.11	–		–	dBm
Maximum output power in 802.11g mode		–		–	dBm
Maximum output power in 802.11n mode		–	13	–	dBm
Transmit spectrum mask					
Margin to 802.11b spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11g spectrum mask		0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit modulation accuracy in 802.11b mode					
1Mbps	As specified in IEEE 802.11b	–	–	35	%
2Mbps		–	–	35	%
5.5Mbps		–	–	35	%
11Mbps		–	–	35	%
Transmit modulation accuracy in 802.11g mode					
6Mbps	As specified in IEEE 802.11g	–	–	–5	dB
9Mbps		–	–	–8	dB
12Mbps		–	–	–10	dB
18Mbps		–	–	–13	dB
24Mbps		–	–	–16	dB
36Mbps		–	–	–19	dB
48Mbps		–	–	–22	dB
54Mbps		–	–	–25	dB
Transmit modulation accuracy in 802.11n mode					
MCS7	As specified in IEEE 802.11n	–	–	–27	dB
Transmit power-on and power-down ramp time in 802.11b mode					
Transmit power-on ramp time from 10% to 90% output power	–	–	–	2	µs
Transmit power-down ramp time from 90% to 10% output power	–	–	–	2	µs

11.6.3 Wi-Fi, 5GHz Receiver RF Specifications

Table 49. Wi-Fi, 5GHZ Receiver RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	4900	–	5845	MHz
Minimum receiver sensitivity in 802.11a mode					
6Mbps	PER < 10%	–	–90	–	dBm
9Mbps		–	–89	–	dBm
12Mbps		–	–88	–	dBm
18Mbps		–	–87	–	dBm
24Mbps		–	–84	–	dBm
36Mbps		–	–80	–	dBm
48Mbps		–	–76	–	dBm
54Mbps		–	–75	–	dBm
Minimum receiver sensitivity in 802.11n (HT-20) mode					
MCS 0	PER < 10%	–	–89	–	dBm
MCS 1		–	–88	–	dBm
MCS 2		–	–85	–	dBm
MCS 3		–	–82	–	dBm
MCS 4		–	–79	–	dBm
MCS 5		–	–75	–	dBm
MCS 6		–	–72	–	dBm
MCS 7		–	–71	–	dBm
Minimum receiver sensitivity in 802.11n (HT-40) mode					
MCS 0	PER < 10%	–	–86	–	dBm
MCS 1		–	–85	–	dBm
MCS 2		–	–83	–	dBm
MCS 3		–	–80	–	dBm
MCS 4		–	–77	–	dBm
MCS 5		–	–73	–	dBm
MCS 6		–	–71	–	dBm
MCS 7		–	–69	–	dBm

11.6.4 Wi-Fi, 5GHz Transmitter RF Specifications

Table 50. Wi-Fi, 5GHz Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	4900		5845	MHz
Linear output power					
Maximum output power in 802.11a mode	54M, UNII-2e	–	13	–	dBm
Maximum output power in 802.11n mode	HT20, MCS7, UNII-2e	–	12	–	dBm
	HT40, MCS7, UNII-2e	–	11	–	dBm
Transmit spectrum mask					
Margin to 802.11a spectrum mask	Maximum output power	0	–	–	dBr
Margin to 802.11n spectrum mask		0	–	–	dBr
Transmit constellation error in 802.11a mode					
54Mbps	As specified in IEEE 802.11n	–	–	–25	dB
Transmit constellation error in 802.11n (HT-20, HT-40) mode					
MCS 7	As specified in IEEE 802.11n	–	–	–27	dB

11.6.5 Bluetooth RF Specifications

Table 51. Bluetooth Receiver RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Sensitivity (BER)	GPSK, BER ≤0.1%	–	–	–	dBm
	π/4-DQPSK, BER ≤ 0.1%	–	–	–	dBm
	BER ≤ 0.1%, 8DPSK	–	–	–	dBm
Maximum Input Level	GPSK, BER ≤0.1%	–20	–	–	dBm
	π/4-DQPSK, BER ≤ 0.1%	–20	–	–	dBm
	BER ≤ 0.1%, 8 DPSK	–20	–	–	dBm
BDR					
Intermodulation Performance	–	–	–	0.1	%
Rx C/I Performance	1DH1	–	–	0.1	%
	1DH3	–	–	0.1	%
	1DH5	–	–	0.1	%
EDR					
Rx C/I Performance	2DH1	–	–	0.1	%
	2DH3	–	–	0.1	%
	2DH5	–	–	0.1	%
	3DH1	–	–	0.1	%
	3DH3	–	–	0.1	%
	3DH5	–	–	0.1	%
Rx BER Floor Performance	BER ≤ 0.001%	–	–	–70	dBm

Table 52. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Output Power (Average)					
BDR (QPSK)	2440 MHz	–		–	dBm
EDR (π/4-DQPSK)	2440 MHz	–		–	dBm
EDR (8DPSK)	2440 MHz	–		–	dBm

Table 53. Bluetooth Low Energy (BLE) RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Rx Receiver Sensitivity PER	At –70dBm	–	–	30.8	%
Rx C/I and Receiver Selectivity Performance PER	–	–	–	30.8	%
Tx Power	–	–		–	dBm

11.6.6 802.15.4 Receiver RF Specifications

The typical numbers indicated in *Table 54* and *Table 55* are one standard deviation below the mean, measured at room temperature 25°C. The Min and Max numbers were measured over process corners at room temperature.

Table 54. 802.15.4 Receiver RF Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Operating Frequency Range	–	2400	–	2483.5	MHz
Receiver Sensitivity PER	At –95dBm	–	–	1	%
Receiver Sensitivity Search	At PER 1%	–	–	–	dBm
Receiver Interference Rejection PER	At –2 Channel, Alternate Channel, 30dB	–	–	1	%
Receiver Interference Rejection PER	At –1 Channel, Adjacent Channel, 0dB	–	–	1	%
Receiver Interference Rejection PER	At +1 Channel, Adjacent Channel, 0dB	–	–	1	%
Receiver Interference Rejection PER	At +2 Channel, Alternate Channel, 30dB	–	–	1	%
Error Vector Magnitude - RMS (EVM)	At Target Power	–	–	30	%
Error Vector Magnitude - Offset (EVM)	At Target Power	–	–	10	%
Receiver Maximum Input Level of Desired Signal	At –20dBm Input	–	–	1	%

Table 55. 802.15.4 Transmitter RF Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power	At highest normal mode power setting			–	dBm
Minimum output power	At lowest power setting	–	–	–	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	–	–	10	%
Carrier frequency error	–	–40	–	+40	ppm
PSD mask relative	3.5 MHz away (Normal)	–20	–	–	dBm
PSD mask absolute	100 KHz BW	–30	–	–	dBm

12 Thermal and Environmental Specifications

12.1 Recommended Operating Conditions

The recommended operation of the ARTIK 530/530s Module is based on the operating conditions listed in *Table 56*.

Table 56. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Main Power Supply	VIN PV:[42,43],PW:[42,43],PY:[42,43],PAA:[42,43],PAB:[42,43]	3.7	4.2	5.0	V
Operating Temperature (ARTIK 530/530s 512 MB)	T_C	–25	–	85	°C
Operating Temperature (ARTIK 530s 1GB)	T_C	0	–	85	°C
Storage Temperature	T_A	–40	–	85 *	°C

*. Flash-based technologies are subject to reduced data retention times at elevated temperatures. Devices should not be stored for extended periods of time at temperatures above 30°C. Devices subject to elevated temperature storage may need to be reflashed.

12.2 Temperature Thresholds for Operating Frequency Throttling

The ARTIK 530/530s Module automatically performs frequency throttling under software control at the thresholds indicated in the following table:

Table 57. Case Temperature vs Maximum Operating Frequency

Temperature	Maximum Operating Frequency
<50°C	1.2 GHz
50° to 60°C	1.0 GHz
60° to 85°C	400 MHz

Module temperatures are dependent on processing load. For high processor loads, these thresholds may be reduced by up to 10 degrees.

For more information, refer to the ARTIK 530 Thermal Guide.

12.3 ESD Ratings

Table 58. ESD Ratings

Symbol	Min.	Max.	Units
ESD stress voltage Human Body Model	–	1	kV

Table 59. Shock and Vibration Ratings

Shock and Vibration		Range
Shock	Packing Drop	75cm (10~19.9Kg) / 91cm (<10Kg)
Vibration	Packing Vibration	0.85Grms/2~200Hz (TTL Grms)

13 Mechanical Specifications

The ARTIK 530/530s Module supports PAD Balls and two RF connectors on a 49mm × 36mm footprint as shown in *Figure 10*. Refer to section *Antenna Connections* for RF connector details. In addition the top view, side view and bottom view with its dimensions can be seen in *Figure 11* and *Figure 12*.

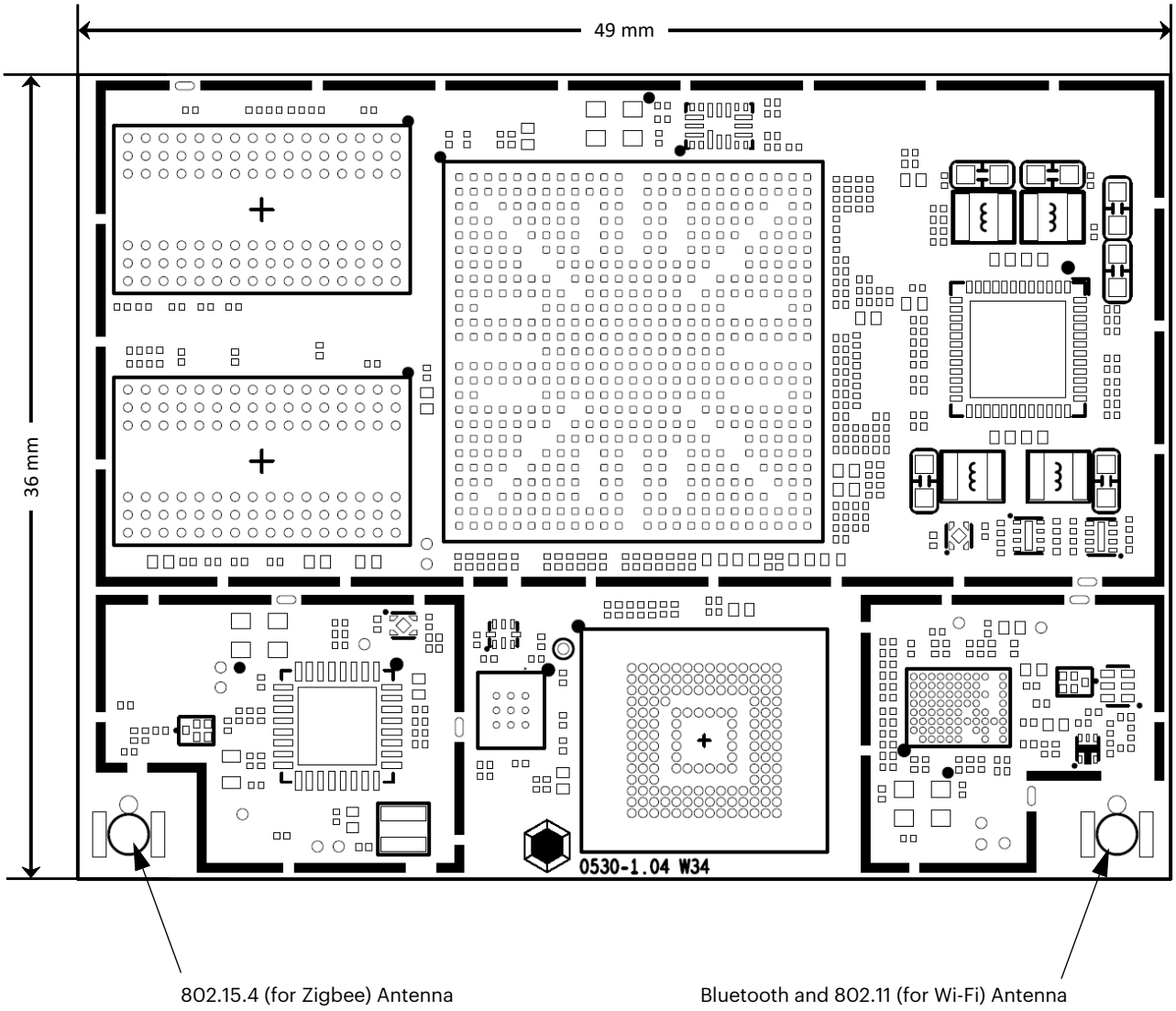

Figure 10. ARTIK 530/530s Module Top View Mechanical Dimensions and Part Location

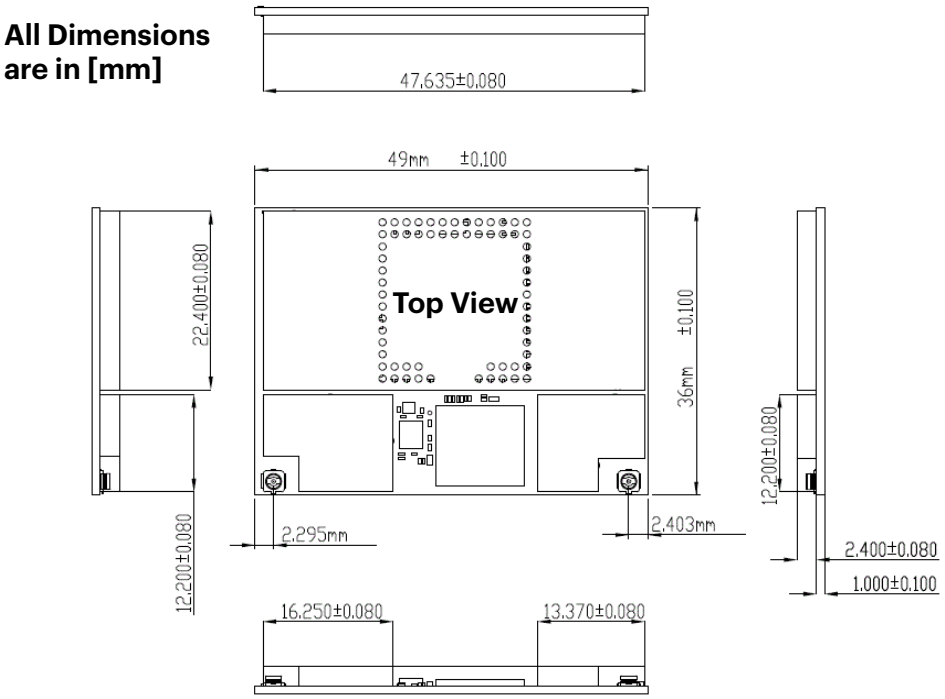

Figure 11. ARTIK 530/530s Module Mechanical Dimensions Top View

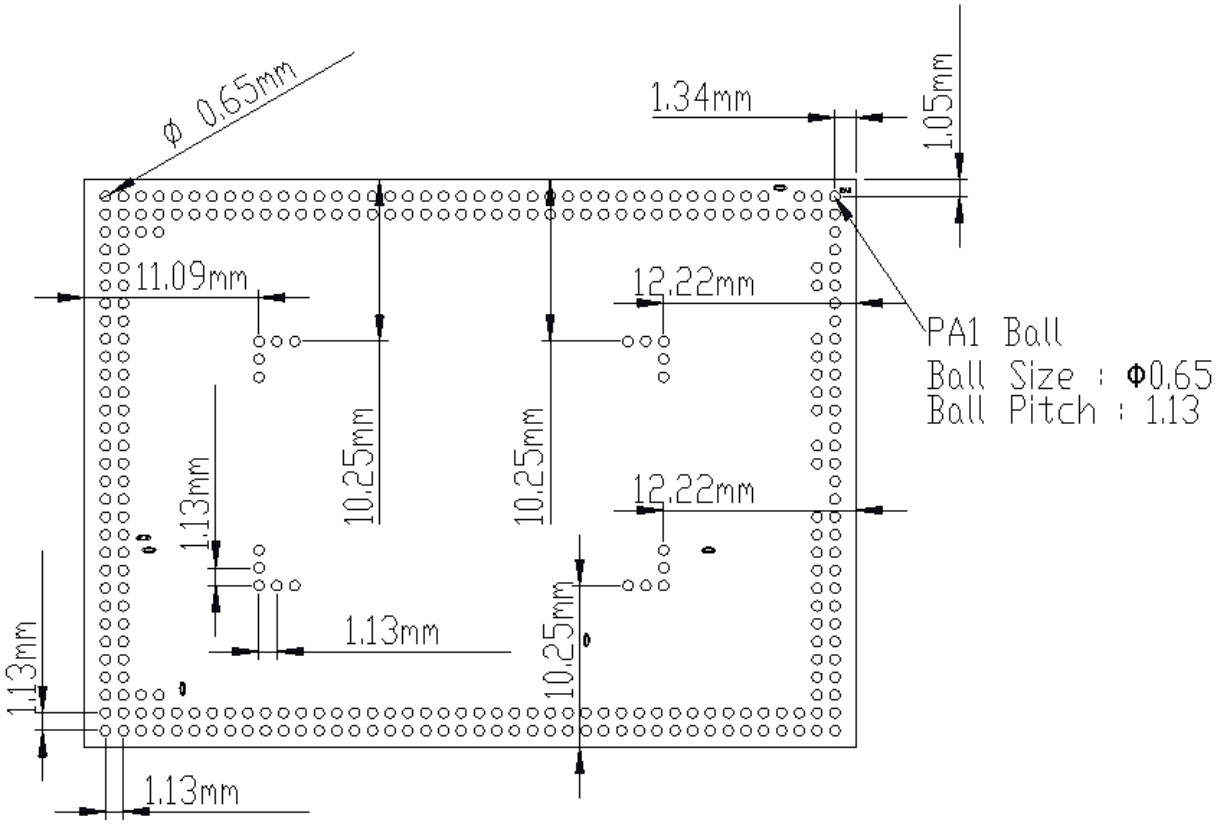

Figure 12. ARTIK 530/530s Module Mechanical Dimensions Bottom View

The inner pin locations on the pad, positioned in an L-shaped form, as depicted in *Figure 13*, are described in *Table 60*.

CAUTION

The inner pads are on a different grid from the outer pads as indicated with the dashed blue lines in *Figure 13*.

CAUTION

The inner pads are *not* horizontally centered in the module

For exact dimensions on ball locations, see *Figure 12*. The locations given in *Table 60* are the absolute coordinates measured from the edge of the ARTIK 530/530s Module to the center of each ball. All inner pads are ground (GND) balls.

Table 60. L-Shaped Ball Locations

Ball Name	X-Location (mm)	Y-Location (mm)
TP282	12.22	25.75
TP283	13.35	25.75
TP284	14.48	25.75
TP285	35.65	25.75
TP286	36.78	25.75
TP287	37.91	25.75
TP288	37.91	24.62
TP289	37.91	23.49
TP290	37.91	12.51
TP291	37.91	11.38
TP292	37.91	10.25
TP293	36.78	10.25
TP294	35.65	10.25
TP295	14.48	10.25
TP296	13.35	10.25
TP297	12.22	10.25
TP298	12.22	11.38
TP299	12.22	12.51
TP300	12.22	23.49
TP301	12.22	24.62

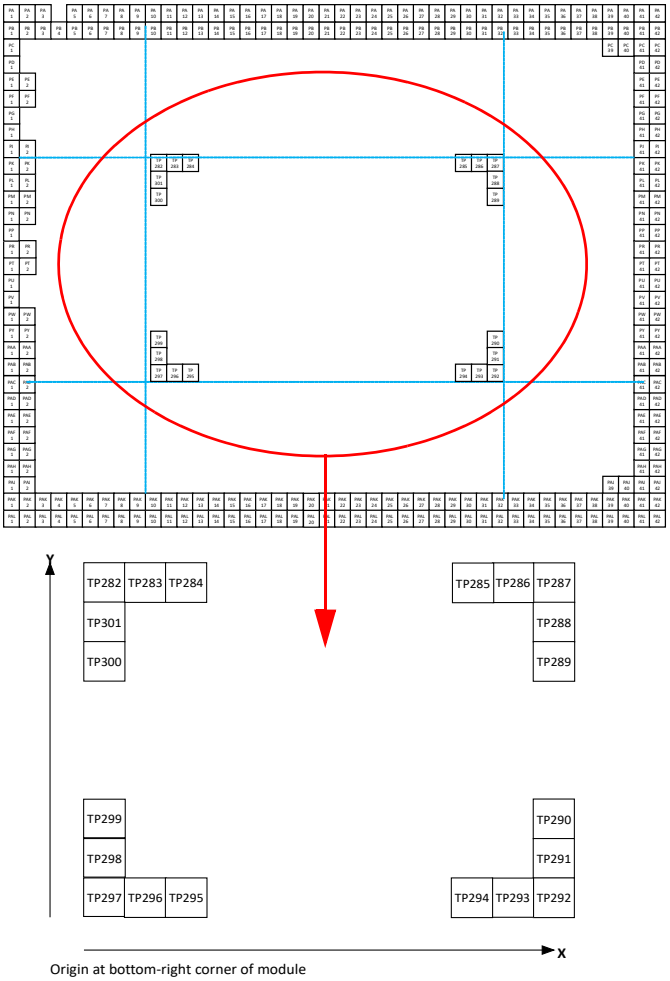

Figure 13. L-Shaped Pad Pins (Top View)

14 Certifications and Compliance

14.1 Bluetooth

The ARTIK 530/530s Module is recognized as a qualified design as set out by the Bluetooth SIG.

Declaration ID: D032725

Qualified Design ID: 88390

14.2 CE

The ARTIK 530/530s Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the Radio Equipment Directive 2014/53/EU. Compliance with the following standards was confirmed:

- Article 3.1a (Health and Safety) — EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2001 + A2:2013
EN62311:2008
- Article 3.1.b (EMC) — EN 301 489-1 V2.1.1, draft EN 301 489-3 V2.1.0
EN 301 489-17 V3.1.1
- Article 3.2 (Radio spectrum use) — EN 300 328 V2.1.1
EN 301 893 V1.8.1 and EN 301 893 V2.1.1 (partial)
EN 300 440 V2.1.1
- Certificate number: — AN17C10983-3 (ARTIK 530 and ARTIK 530s)
AN17C11024-1 (ARTIK 530s 1G)

For a formal notified body statement of opinion contact your sales representative.

14.3 FCC

The ARTIK 530/530s Module complies with the following two sections (15C and 15E) of Part 15 of the FCC rules namely:

- Spread spectrum transmitter (SST) compliance (15C):
  - 2402–2480MHz frequency range, output power 0.0049W
- Digital transmission system (DTS) compliance (15C):
  - 2402–2480MHz frequency range, output power 0.004W
  - 2405–2475MHz frequency range, output power 0.0412W
  - 2412–2462MHz frequency range, output power 0.0308W
- Unlicensed national information infrastructure TX compliance (15E) in the:
  - 5180-5240MHz frequency range, output power 0.0206W
  - 5260-5320MHz frequency range, output power 0.0221W
  - 5500-5720MHz frequency range, output power 0.0222W
  - 5745-5825MHz frequency range, output power 0.01W

FCC Identifier: A3LSIP005AFS30

Modular Type: Limited Single Modular

14.4 IC

The ARTIK 530/530s Module complies with the IC license–exempt RSS standard.

Radio certification number: 649E-SIP005AFS30

14.5 KCC

The ARTIK 530/530s Module complies with the standards set by the Korean communications commission (KCC).

ARTIK 530/530s Module KCC Identifier: MSIP-CRM-SEC-SIP005AFS30

14.6 SRRC

Both the ARTIK 530/530s Module and the ARTIK 530/530s Development Kit comply with the standards set by the People's Republic of China.

CMIIT ID: 2017AJ3123 (M)(ARTIK 530/530s Module)

CMIIT ID: 2017AJ2921 (ARTIK 530/530s Development Kit)

14.7 HDMI Compliance

The ARTIK 530/530s Module passed the self-test, HDMI CTS version 1.4b on 8/26/2016 provided by HDMI Licensing LLC.

14.8 RoHS Compliance

The ARTIK 530/530s Module complies with the hazardous substance limits of directive 2011/65/EU and the conformity assessment procedure as outlined in Decision 768/2008/EC, Annex II, Module A, Point 2, as well as RoHS harmonized standard EN 50581.

Report reference number: F690101/LF-CTSAYGU16-06911

14.9 FCC Regulatory Disclosures

This device complies with Part 15 of the FCC`s Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesirable operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the transmitter's radiating structure(s) and the body of the user or nearby persons.

This module is intended for OEM integration. The OEM integrator is responsible for FCC compliance and compliance with all applicable regulations including those for modular transmitters 47 C.F.R. 15.212. The OEM product must comply with all applicable labeling requirements including those contained in 15 C.F.R. 15.19. The OEM is solely responsible for certification and testing and labeling of its own products. In addition to any independently required labels, the OEM shall also affix to the outside of a device into which the module is installed a label referring to the enclosed module. This exterior label should be prepared in a legible font and permanently affixed and using the wording "Contains Transmitter Module FCCID: A3LSIP005AFS30"

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

The OEM shall require that the end user of its product be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The OEM shall further inform its end user that any change or modifications to this module not expressly approved by the manufacturer will void the warranty and the users' authority to operate the equipment.

14.10 Industry Canada Regulatory Disclosures

14.10.1 Industry Canada Statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'opération est soumise aux deux conditions suivantes:(1) cet appareil ne peut causer d'interférences, et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

Industry Canada Radiation Exposure Statement and Limitations on Use

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body. This equipment should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

This equipment is restricted to indoor use in the 5.15-5.25 GHz range. This equipment is not able to be operated at 5600-5650. In the United States and Canada, only Channel 1~11 can be operated and these channel assignments deal only with the 2.4 GHz range.

The end product must be labeled to display the Industry Canada certification number of the module.

"Contains transmitter module IC: 649E-SIP005AFS30"

Le dispositif d'accueil doivent être étiquetés pour afficher le numéro de certification d'Industrie Canada du module.
"Contient module émetteur IC : 649E-SIP005AFS30"

14.11 EU Regulatory Disclosures

14.11.1 Statement*

The following statement must be supplied with each product but can be printed in the user manual, the packaging, or provided as a separated leaflet.

> Hereby, Samsung declares that this IoT Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the Radio Equipment Directive 2014/53/EU and RoHS directive 2011/65/EU.
>
> "The declaration of conformity may be consulted at [www.artik.io/certification]"

The 5150 - 5350 MHz and 5470 - 5725 MHz bands are for indoor use only.

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

15 Ordering Information

Item	Order Number	Description
ARTIK 530 Module	SIP-005AFS301	–
ARTIK 530s Module	SIP-005AFS302	Includes 512MB DRAM
ARTIK 530s 1G Module	SIP-005AUS332	Includes 1GB DRAM
ARTIK 530 Development Kit	SIP-KITNXD001	ARTIK 530 Development Module ARTIK 530/530s Interposer Board Platform Board Interface Board Two Antennas (one 802.15.4, one BT/Wi-Fi)
ARTIK 530s Development Kit	SIP-KITNXD002	ARTIK 530s Development Module ARTIK 530/530s Interposer Board Platform Board Interface Board Two Antennas (one 802.15.4, one BT/Wi-Fi)
ARTIK 530s 1G Development Kit	SIP-KITNXG002	ARTIK 530s 1G Development Module ARTIK 530/530s Interposer Board Platform Board Interface Board Two Antennas (one 802.15.4, one BT/Wi-Fi)

For volume ordering of evaluation kits, contact a sales representative in your area or email sales@artik.io.

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